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UNIVERSITÀ DI ROMA

ALLEGATO 1

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**FACOLTÀ DI INGEGNERIA DELL'INFORMAZIONE, INFORMATICA E
STATISTICA**

**ESAMI DI STATO PER L'ABILITAZIONE ALLA PROFESSIONE DI
INGEGNERE DELL'INFORMAZIONE**

II SESSIONE – NOVEMBRE 2025

SEZIONE A

PRIMA PROVA SCRITTA

TRACCIA 1

Si discuta, con riferimento a uno o più ambiti di interesse o competenza, il ruolo che l'ingegnere dell'informazione è chiamato a svolgere alla luce degli attuali sviluppi della società e delle aspettative derivanti dalle conoscenze e competenze acquisite nel proprio percorso formativo.



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ALLEGATO 2

**FACOLTÀ DI INGEGNERIA DELL'INFORMAZIONE, INFORMATICA E
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II SESSIONE – NOVEMBRE 2025

SEZIONE A

PRIMA PROVA SCRITTA

TRACCIA 2

Le tecnologie dell'informazione si fondano sull'evoluzione di due ambiti complementari: le tecnologie dei dispositivi fisici e dei componenti materiali, e le metodologie e procedure che ne guidano l'utilizzo e l'integrazione.

Si discuta, sulla base della propria esperienza e degli studi condotti, l'influenza reciproca tra questi due comparti, valutando in che misura gli sviluppi di uno possano condizionare o favorire quelli dell'altro, fino a ipotizzare eventuali forme di "primazia".



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

SEZIONE A SECONDA PROVA SCRITTA

INGEGNERIA BIOMEDICA

TRACCIA 1

Al giorno d'oggi i sensori si stanno affermando sempre più come dispositivi elettronici fondamentali per l'interazione umana con l'ambiente circostante. Si analizzi la catena di acquisizione del segnale approfondendo i parametri fondamentali che definiscono le prestazioni di un sensore e i requisiti critici richiesti ai relativi circuiti elettronici di lettura. Si riporti, inoltre, un esempio di applicazione nel settore biomedicale.

Mm
Q
ff
gk
P



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

SEZIONE A SECONDA PROVA SCRITTA

INGEGNERIA BIOMEDICA

TRACCIA 2

Il candidato illustri il ruolo dell'imaging biomedico, descrivendone i diversi campi di applicazione. Con riferimento a uno specifico esempio di tecnica di imaging, ne analizzi i limiti e tecnologici in termini di parametri caratterizzanti la tecnica considerata, e illustri le principali sfide ingegneristiche per la sua evoluzione.

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II SESSIONE – NOVEMBRE 2025

SEZIONE A

SECONDA PROVA SCRITTA

**INGEGNERIA GESTIONALE
LM-31**

TRACCIA 1

Si discuta il concetto di Rischio come inteso in ambito economico-gestionale, così come il concetto di Resilienza Organizzativa.

Si descriva il processo di Gestione dei Rischi di Progetto (Project Risk Management), avendo cura di evidenziarne le varie fasi. Per ogni fase, si facciano esempi di strumenti, metodi e pratiche utilizzati. Si esemplifichi anche l'applicazione del processo in uno o più casi reali.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

SECONDA PROVA SCRITTA

**INGEGNERIA GESTIONALE
LM-31**

TRACCIA 2

Si discuta il concetto di Costo e le sue declinazioni in ambito economico-gestionale.
Si descriva il processo di Gestione dei Costi di Progetto (Project Cost Management), avendo cura di evidenziarne le varie fasi. Per ogni fase, si facciano esempi di strumenti, metodi e pratiche utilizzati. Si esemplifichi anche l'applicazione del processo in uno o più casi reali.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

SECONDA PROVA SCRITTA

INGEGNERIA INFORMATICA

TRACCIA 1

In base alle conoscenze acquisite il candidato presenti il processo di sviluppo del software e ne presenti le metodologie, gli standard di qualità, le metriche e le tecniche comunemente usate per la stima economica, la pianificazione ed il test di applicazioni software di qualità professionale.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

SECONDA PROVA SCRITTA

INGEGNERIA INFORMATICA

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TRACCIA 2

In base alle conoscenze acquisite, il candidato illustri i principali principi della sicurezza informatica, in particolare confidenzialità, integrità e disponibilità. Il candidato descriva come le tecniche e gli algoritmi crittografici possano essere impiegati per garantire tali principi, evidenziandone il ruolo nei sistemi informatici e fornendo, ove opportuno, esempi di applicazioni pratiche.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

SECONDA PROVA SCRITTA

INTELLIGENZA ARTIFICIALE E ROBOTICA

TRACCIA 1

In base alle conoscenze acquisite, il candidato discuta i fondamenti della visione artificiale e il ruolo che essa riveste nella progettazione di sistemi autonomi per l'interpretazione e la ricostruzione di una scena a partire da immagini e video. Il candidato presenti le metodologie principali per il riconoscimento e la segmentazione di immagini e video, con particolare riferimento agli approcci basati sull'apprendimento automatico e sull'apprendimento profondo, discutendone vantaggi e limiti.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

SECONDA PROVA SCRITTA

INTELLIGENZA ARTIFICIALE E ROBOTICA

TRACCIA 2

In base alle conoscenze acquisite, il candidato descriva i fondamenti della robotica e le principali problematiche legate al controllo del movimento di manipolatori robotici. Il candidato illustri l'architettura di un sistema robotico, analizzando componenti di attuazione e sensoriali, e discuta i metodi di base per la modellistica e l'analisi cinematica. Vengano inoltre presentati i principali algoritmi per la pianificazione e la programmazione dei movimenti, con particolare riferimento alla pianificazione delle traiettorie e al controllo cinematico, discutendone l'impiego in dispositivi di guida autonoma.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

**SECONDA PROVA SCRITTA
SEZIONE A**

INGEGNERIA DELLE TELECOMUNICAZIONI

TRACCIA 1

L'utilizzo di una risorsa condivisa tra gli utenti di una rete richiede l'introduzione di tecniche di accesso multiplo che permettano una suddivisione efficiente della risorsa stessa. In tale ottica i sistemi di accesso multiplo più comuni operano in uno dei tre seguenti modi: a divisione di tempo, a divisione di frequenza ed a divisione di codice. Il candidato esponga le caratteristiche delle tecniche di accesso sopra citate mettendo in evidenza quali siano le differenze tra tali tecniche, ed indicando uno o più esempi di applicazione di una delle tecniche in sistemi di telecomunicazione di propria conoscenza.

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II SESSIONE – NOVEMBRE 2025

SEZIONE A

**SECONDA PROVA SCRITTA
SEZIONE A**

INGEGNERIA DELLE TELECOMUNICAZIONI

TRACCIA 2

Un sistema di telecomunicazione richiede che l'informazione venga trasferita attraverso un mezzo trasmissivo di tipo fisico, sia esso in rame (doppino o cavo coassiale), in fibra ottica, o facente uso di segnali radio (trasmissione di tipo "wireless"). Il candidato esponga le caratteristiche delle tre tipologie di mezzi trasmissivi sopra citati mettendo in evidenza quali siano le prestazioni che tali mezzi offrono, le problematiche che sono connesse all'utilizzo di tali mezzi anche dal punto di vista delle sorgenti e dei ricevitori che devono essere utilizzati.



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II SESSIONE – LUGLIO 2025

SEZIONE A

PROVA PRATICA

**INGEGNERIA GESTIONALE
LM-31**

TRACCIA 1

Un sistema produttivo alimenta un impianto a valle alternando durante la giornata, e sullo stesso macchinario, la produzione di:

- 5 lotti di prodotto A
- 7 lotti di prodotto B
- 8 lotti di prodotto C

Il tempo di setup necessario prima dell'avvio di ciascun lotto è di:

- 8 minuti per il prodotto A
- 7 minuti per il prodotto B
- 3 minuti per il prodotto C

La lavorazione di un lotto del prodotto A dura 45 minuti e produce 45 pezzi.

La lavorazione di un lotto del prodotto B dura 40 minuti e produce 20 pezzi.

La lavorazione di un lotto del prodotto C dura 40 minuti e produce 20 pezzi.

La lavorazione è organizzata in tre turni di 8 ore ciascuno, serviti da tre operai (uno per turno). In ciascun turno restano quindi non utilizzate sia manodopera diretta che ore macchina. Calcolare i costi delle attività descritte e il loro impatto sul costo unitario dei tre beni. Si consideri un ammortamento annuo dei macchinari di 180.000€ e un costo annuo di un operaio di 35.000€. L'impianto è attivo per 360 giorni all'anno. Si ignorino tutte le voci di costo non esplicitamente menzionate nel testo. Si considerino come costi di periodo quelli relativi alle risorse non utilizzate.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

PROVA PRATICA

INTELLIGENZA ARTIFICIALE E ROBOTICA

TRACCIA 1

Si vuole realizzare un sistema di collision avoidance per autovetture che tenga conto sia di eventuali altri mezzi nella carreggiata stradale che della presenza di pedoni che potrebbero impegnare la carreggiata improvvisamente.

Il sistema deve offrire le seguenti funzionalità:

- mantenere una distanza di sicurezza preimpostata dal mezzo che lo precede, rallentando se necessario al fine di mantenere la distanza eventualmente anche arrivando a fermarla
- permettere di ridurre tale distanza fino alla metà in fase di sorpasso (il sorpasso avviene mentre il mezzo non diminuisce la propria velocità e la freccia sinistra è inserita)
- allertare il guidatore della presenza di pedoni pericolosamente vicini alla carreggiata stradale
- rallentare ed eventualmente fermare la macchina se un pedone invade la carreggiata

Si chiede al candidato di progettare il sistema sopra descritto, mostrando:

- i principali casi d'uso;
- uno schema architetturale che includa una descrizione logica dell'hardware utilizzato (sensori e attuatori), dei principali moduli software e di come essi comunichino;



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- la tecnologia scelta per ciascuno dei moduli sopra indicati;
- i documenti di progetto (diagrammi UML), opportunamente commentati.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

PROVA PRATICA

INGEGNERIA INFORMATICA

TRACCIA 1

Una federazione sportiva intende realizzare un sistema informatico per la gestione di un campionato di basket, con l'obiettivo di organizzare le informazioni relative alle squadre partecipanti, agli incontri disputati e all'andamento del campionato nel corso della stagione.

Il sistema dovrà supportare l'intero svolgimento del campionato, dalla fase di organizzazione iniziale fino alla consultazione dei risultati e della classifica finale. In particolare, dovrà consentire la gestione delle partite, l'inserimento dei risultati e l'elaborazione automatica delle informazioni necessarie per valutare le prestazioni delle squadre.

Il sistema deve essere consultabile sia tramite interfaccia web che tramite applicazione dedicata.

Considerata la possibilità che i requisiti del sistema evolvano nel tempo (ad esempio modifiche al regolamento del campionato, nuove modalità di consultazione dei dati o richieste di funzionalità aggiuntive), il sistema deve venire sviluppato seguendo un approccio di progettazione agile, basato su rilasci incrementali e sull'evoluzione progressiva della soluzione.

Il candidato dovrà:

1. Fornire un'analisi del problema e dei requisiti



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2. Individuare e descrivere le entità coinvolte, le loro caratteristiche e le relazioni significative tramite
3. Progettare il modello dei dati, illustrando la struttura logica adottata e motivando le scelte effettuate in relazione all'approccio agile.
4. Descrivere l'architettura complessiva del sistema, includendo le modalità di accesso tramite interfaccia web e applicazione dedicata, nonché le principali tecnologie e strumenti utilizzati.
5. Produrre un piano dei test.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

PROVA PRATICA

Ingegneria delle Comunicazioni

TRACCIA 1

Si supponga di dover dimensionare un collegamento radio tra un terminale mobile a bordo di un veicolo ed una stazione radio base.

Il collegamento è utilizzato per trasferire un segnale video in bianco e nero a bassa risoluzione, caratterizzato da una frequenza di quadro (cioè il numero di immagini generate al secondo) pari a $f_q = 15$ quadri/sec. Ognuna delle immagini da trasmettere è rappresentata da 120 righe, ed ogni riga è rappresentata da 160 campioni. Ogni campione è rappresentato utilizzando 4 bit. Il flusso binario così ottenuto è posto in ingresso ad un modulatore multilivello ad L livelli, ed il segnale multilivello di banda base in uscita da tale modulatore è quindi portato a radiofrequenza attraverso una modulazione di ampiezza analogica.

Le specifiche del sistema richiedono che la probabilità di errore sul collegamento sia non superiore a 10^{-6} ($\gamma^2=10.5$ dB) quando il veicolo si trova a una distanza $d = 6$ km dalla stazione base.

Sapendo che la modulazione utilizzata è di tipo Banda Laterale Doppia – Portante Soppressa (BLD-PS) intorno a una frequenza portante $f_p = 3.5$ GHz, e che l'occupazione di banda totale a radiofrequenza è pari a $B_{RF} = 576$ kHz si chiede di:

1. calcolare la velocità di trasmissione binaria R_b del segnale video da trasmettere;
2. calcolare il numero di livelli L in trasmissione, assumendo un valore di roll-off γ pari a 0;
3. determinare l'attenuazione subita dal segnale lungo il collegamento, esprimendola in dB;
4. calcolare l'SNR dopo demodulazione necessario per garantire le prestazioni richieste;
5. determinare la minima potenza necessaria in trasmissione per rispettare le specifiche, nel caso di antenne trasmittente e ricevente isotrope ed a temperatura $T_A=T_0$, e sapendo che il ricevitore ha una figura di rumore complessiva $F = 4$ dB.

Il flusso binario a velocità R_b ottenuto alla stazione radio base in uscita dal ricevitore viene moltiplicato con altri flussi binari provenienti da altre sorgenti ottenendo un nuovo flusso binario a velocità $R_{b2} = 100$ Mb/s che viene trasmesso attraverso un ponte radio che si estende su una tratta di lunghezza $d = 12$ km. Tale flusso è inviato in ingresso ad un modulatore multilivello ad $L=8$ livelli e quindi portato a radiofrequenza adottando uno schema di modulazione di



ampiezza analogica di tipo Banda Laterale Unica – Portante Soppressa (BLU-PS). La frequenza portante vale $f_p = 18$ GHz. In trasmissione è utilizzato un filtro a coseno rialzato con fattore di roll-off $\gamma = 0.2$. Le antenne in trasmissione e in ricezione hanno entrambe un guadagno $G = 10$ dB. Il fattore di rumore complessivo caratterizzante il ricevitore utilizzato ha valore $F_{dB} = 6$ dB. Si desidera ottenere una probabilità di errore sul simbolo non superiore a $P_e = 10^{-5}$ (corrispondente a $\gamma^2 = 9.8$ dB).

6. Calcolare la minima potenza in ricezione W_{Rmin} necessaria affinché la specifica sulla probabilità di errore possa essere rispettata.
7. Calcolare la minima potenza in trasmissione W_{Tmin} che permette il rispetto delle specifiche di sistema.
8. Calcolare, nel caso in cui l'effettiva potenza trasmessa risulti essere $W_T = 3 * W_{Tmin}$, il valore del margine M introdotto nel sistema.
9. Si determini se in presenza di una precipitazione piovosa di intensità $r = 5$ mm/h il sistema è fuori servizio o meno (si utilizzi per il calcolo dell'attenuazione supplementare dovuta a pioggia espressa in dB il modello ITU PN.838: $A_{SdB} = Kr^\alpha d_{Km}$. Si assuma per tale modello $K=0.1$ e $\alpha=1.1$.)
10. Assumendo che l'intensità di precipitazione r della pioggia abbia una funzione di densità di probabilità pari a:

$$p(r) = \begin{cases} 0 & r \leq 0 \\ e^{-r} & r > 0 \end{cases}$$

si calcoli la probabilità di fuori servizio P_{fs} e si determini il numero di minuti/mese in cui il sistema è fuori specifica.



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II SESSIONE – NOVEMBRE 2025

SEZIONE A

PROVA PRATICA

INGEGNERIA BIOMEDICA – LM-29

TRACCIA 1

Al giorno d'oggi i sensori si stanno affermando sempre più come dispositivi elettronici fondamentali per l'interazione umana con l'ambiente circostante. Si analizzi la catena di acquisizione del segnale approfondendo i parametri fondamentali che definiscono le prestazioni di un sensore e i requisiti critici richiesti ai relativi circuiti elettronici di lettura. Si riporti, inoltre, un esempio di applicazione nel settore biomedicale.

FEATURES

Easy to use

Gain set with one external resistor
(Gain range 1 to 10,000)

Wide power supply range ($\pm 2.3\text{ V}$ to $\pm 18\text{ V}$)

Higher performance than 3 op amp IA designs

Available in 8-lead DIP and SOIC packaging

Low power, 1.3 mA max supply current

Excellent dc performance (B grade)

50 μV max, input offset voltage

0.6 $\mu\text{V}/^\circ\text{C}$ max, input offset drift

1.0 nA max, input bias current

100 dB min common-mode rejection ratio ($G = 10$)

Low noise

9 nV/ $\sqrt{\text{Hz}}$ @ 1 kHz, input voltage noise

0.28 μV p-p noise (0.1 Hz to 10 Hz)

Excellent ac specifications

120 kHz bandwidth ($G = 100$)

15 μs settling time to 0.01%

APPLICATIONS

Weigh scales

ECG and medical instrumentation

Transducer interface

Data acquisition systems

Industrial process controls

Battery-powered and portable equipment

CONNECTION DIAGRAM

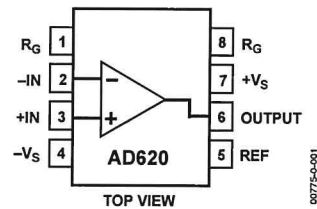


Figure 1. 8-Lead PDIP (N), CERDIP (Q), and SOIC (R) Packages

PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs and offers lower power (only 1.3 mA max supply current), making it a good fit for battery-powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max, and offset drift of 0.6 $\mu\text{V}/^\circ\text{C}$ max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications, such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superbeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/ $\sqrt{\text{Hz}}$ at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, and 0.1 pA/ $\sqrt{\text{Hz}}$ input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01%, and its cost is low enough to enable designs with one in-amp per channel.

Table 1. Next Generation Upgrades for AD620

Part	Comment
AD8221	Better specs at lower price
AD8222	Dual channel or differential out
AD8226	Low power, wide input range
AD8220	JFET input
AD8228	Best gain accuracy
AD8295	+2 precision op amps or differential out
AD8429	Ultra low noise

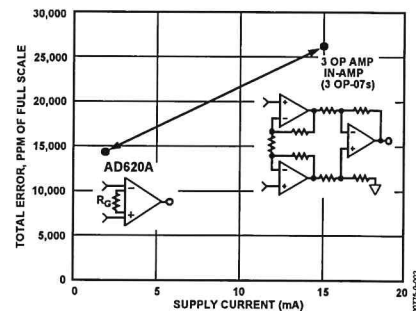


Figure 2. Three Op Amp IA Designs vs. AD620

Rev. H

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AD620

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		Removed AD620CHIPS from ORDERING GUIDE	4
		Removed METALLIZATION PHOTOGRAPH.....	4
12/04—Rev. F to Rev. G		Replaced TPCs 1–3	5
Updated Format.....	Universal	Replaced TPC 12.....	6
Change to Features.....	1	Replaced TPC 30.....	9
Change to Product Description.....	1	Replaced TPCs 31 and 32.....	10
Changes to Specifications.....	3	Replaced Figure 4.....	10
Added Metallization Photograph.....	4	Changes to Table I.....	11
Replaced Figure 4-Figure 6	6	Changes to Figures 6 and 7	12
Replaced Figure 15	7	Changes to Figure 8	13
Replaced Figure 33	10	Edited INPUT PROTECTION section.....	13
Replaced Figure 34 and Figure 35.....	10	Added new Figure 9	13
Replaced Figure 37.....	10	Changes to RF INTERFACE section	14
Changes to Table 3	13	Edit to GROUND RETURNS FOR INPUT BIAS CURRENTS section.....	15
Changes to Figure 41 and Figure 42	14	Updated OUTLINE DIMENSIONS	16
Changes to Figure 43	15		
Change to Figure 44.....	17		

SPECIFICATIONS

Typical @ 25°C, $V_S = \pm 15$ V, and $R_L = 2$ k Ω , unless otherwise noted.

Table 2.

Parameter	Conditions	AD620A		AD620B		AD620S ¹		Unit		
		Min	Typ	Max	Min	Typ	Max		Min	Typ
GAIN	$G = 1 + (49.4 \text{ k}\Omega/R_G)$									
Gain Range		1		10,000	1		10,000	1		10,000
Gain Error ²	$V_{OUT} = \pm 10$ V									
G = 1			0.03	0.10		0.01	0.02		0.03	0.10
G = 10			0.15	0.30		0.10	0.15		0.15	0.30
G = 100			0.15	0.30		0.10	0.15		0.15	0.30
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70
Nonlinearity	$V_{OUT} = -10$ V to $+10$ V									
G = 1–1000	$R_L = 10$ k Ω		10	40		10	40		10	40
G = 1–100	$R_L = 2$ k Ω		10	95		10	95		10	95
Gain vs. Temperature	G = 1			10			10			10
	Gain > 1 ²			–50			–50			–50
VOLTAGE OFFSET	(Total RTI Error = $V_{OSI} + V_{OSO}/G$)									
Input Offset, V_{OSI}	$V_S = \pm 5$ V to ± 15 V		30	125		15	50		30	125
Overtemperature	$V_S = \pm 5$ V to ± 15 V			185			85			225
Average TC	$V_S = \pm 5$ V to ± 15 V		0.3	1.0		0.1	0.6		0.3	1.0
Output Offset, V_{OSO}	$V_S = \pm 15$ V		400	1000		200	500		400	1000
Overtemperature	$V_S = \pm 5$ V to ± 15 V			1500			750			1500
Average TC	$V_S = \pm 5$ V to ± 15 V		5.0	15		2.5	7.0		5.0	15
Offset Referred to the Input vs. Supply (PSR)	$V_S = \pm 2.3$ V to ± 18 V									
G = 1		80	100		80	100		80	100	
G = 10		95	120		100	120		95	120	
G = 100		110	140		120	140		110	140	
G = 1000		110	140		120	140		110	140	
INPUT CURRENT										
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2
Overtemperature				2.5			1.5			4
Average TC			3.0			3.0			8.0	
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0
Overtemperature				1.5			0.75			2.0
Average TC			1.5			1.5			8.0	
INPUT										
Input Impedance										
Differential			10 2			10 2			10 2	
Common-Mode			10 2			10 2			10 2	
Input Voltage Range ³	$V_S = \pm 2.3$ V to ± 5 V	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$
Overtemperature	$V_S = \pm 5$ V to ± 18 V	$-V_S + 2.1$		$+V_S - 1.3$	$-V_S + 2.1$		$+V_S - 1.3$	$-V_S + 2.1$		$+V_S - 1.3$
		$-V_S + 1.9$		$+V_S - 1.4$	$-V_S + 1.9$		$+V_S - 1.4$	$-V_S + 1.9$		$+V_S - 1.4$
Overtemperature		$-V_S + 2.1$		$+V_S - 1.4$	$-V_S + 2.1$		$+V_S + 2.1$	$-V_S + 2.3$		$+V_S - 1.4$

AD620

Parameter	Conditions	AD620A			AD620B			AD620S ¹			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Common-Mode Rejection											
Ratio DC to 60 Hz with 1 kΩ Source Imbalance	$V_{CM} = 0\text{ V to } \pm 10\text{ V}$										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	$R_L = 10\text{ k}\Omega$ $V_S = \pm 2.3\text{ V}$ to $\pm 5\text{ V}$	$-V_S + 1.1$	$+V_S - 1.2$		$-V_S + 1.1$	$+V_S - 1.2$		$-V_S + 1.1$	$+V_S - 1.2$		V
Overtemperature	$V_S = \pm 5\text{ V}$ to $\pm 18\text{ V}$	$-V_S + 1.4$	$+V_S - 1.3$		$-V_S + 1.4$	$+V_S - 1.3$		$-V_S + 1.6$	$+V_S - 1.3$		V
Overtemperature Short Circuit Current		$-V_S + 1.2$	$+V_S - 1.4$		$-V_S + 1.2$	$+V_S - 1.4$		$-V_S + 1.2$	$+V_S - 1.4$		V
		$-V_S + 1.6$	$+V_S - 1.5$		$-V_S + 1.6$	$+V_S - 1.5$		$-V_S + 2.3$	$+V_S - 1.5$		V
			± 18			± 18			± 18		mA
DYNAMIC RESPONSE											
Small Signal -3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/ μs
Settling Time to 0.01%	10 V Step										
G = 1-100			15			15			15		μs
G = 1000			150			150			150		μs
NOISE											
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e_{ni}^2) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/ $\sqrt{\text{Hz}}$
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/ $\sqrt{\text{Hz}}$
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	$\mu\text{V p-p}$
G = 10			0.55			0.55	0.8		0.55	0.8	$\mu\text{V p-p}$
G = 100-1000			0.28			0.28	0.4		0.28	0.4	$\mu\text{V p-p}$
Current Noise	$f = 1\text{ kHz}$		100			100			100		fA/ $\sqrt{\text{Hz}}$
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}	$V_{IN+}, V_{REF} = 0$		20			20			20		kΩ
I_{IN}			50	60		50	60		50	60	μA
Voltage Range		$-V_S + 1.6$	$+V_S - 1.6$		$-V_S + 1.6$	$+V_S - 1.6$		$-V_S + 1.6$	$+V_S - 1.6$		V
Gain to Output		1 ± 0.0001			1 ± 0.0001			1 ± 0.0001			
POWER SUPPLY											
Operating Range ⁴		± 2.3	± 18		± 2.3	± 18		± 2.3	± 18		V
Quiescent Current	$V_S = \pm 2.3\text{ V}$ to $\pm 18\text{ V}$		0.9	1.3		0.9	1.3		0.9	1.3	mA
Overtemperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance		-40 to $+85$			-40 to $+85$			-55 to $+125$			$^{\circ}\text{C}$

¹ See Analog Devices military data sheet for 883B tested specifications.

² Does not include effects of external resistor R_G .

³ One input grounded. $G = 1$.

⁴ This is defined as the same supply range that is used to specify PSR.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	± 18 V
Internal Power Dissipation ¹	650 mW
Input Voltage (Common-Mode)	$\pm V_S$
Differential Input Voltage	25 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range (Q)	-65°C to $+150^{\circ}\text{C}$
Storage Temperature Range (N, R)	-65°C to $+125^{\circ}\text{C}$
Operating Temperature Range	
AD620 (A, B)	-40°C to $+85^{\circ}\text{C}$
AD620 (S)	-55°C to $+125^{\circ}\text{C}$
Lead Temperature Range (Soldering 10 seconds)	300°C

¹ Specification is for device in free air:
 8-Lead Plastic Package: $\theta_{JA} = 95^{\circ}\text{C}$
 8-Lead CERDIP Package: $\theta_{JA} = 110^{\circ}\text{C}$
 8-Lead SOIC Package: $\theta_{JA} = 155^{\circ}\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

(@ 25°C, $V_S = \pm 15\text{ V}$, $R_L = 2\text{ k}\Omega$, unless otherwise noted.)

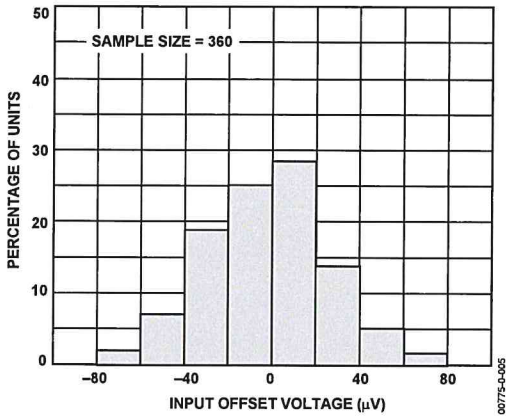


Figure 3. Typical Distribution of Input Offset Voltage

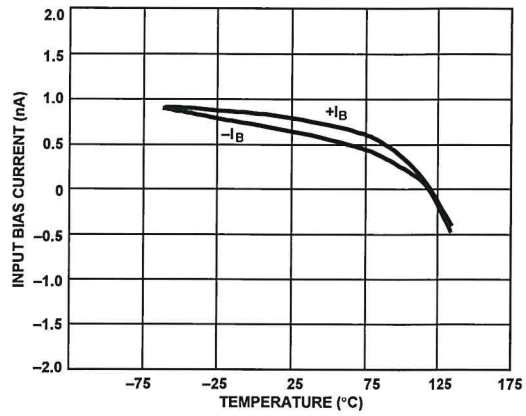


Figure 6. Input Bias Current vs. Temperature

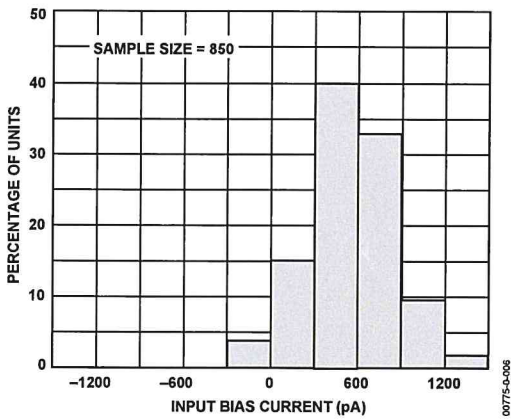


Figure 4. Typical Distribution of Input Bias Current

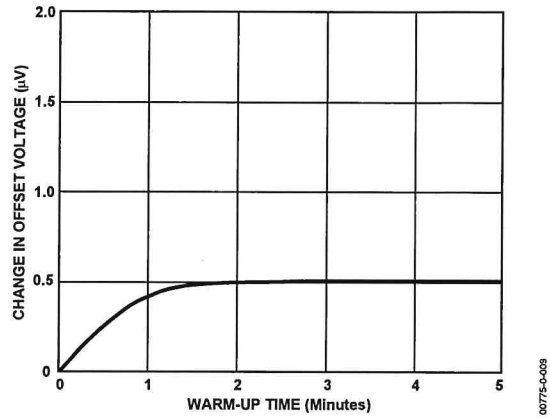


Figure 7. Change in Input Offset Voltage vs. Warm-Up Time

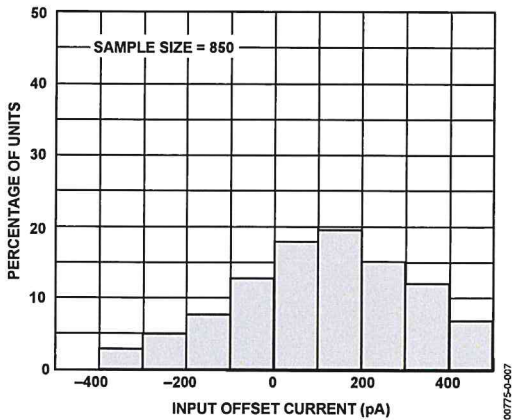


Figure 5. Typical Distribution of Input Offset Current

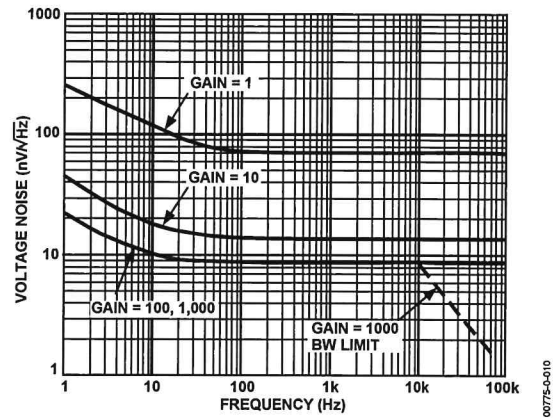


Figure 8. Voltage Noise Spectral Density vs. Frequency ($G = 1 - 1000$)

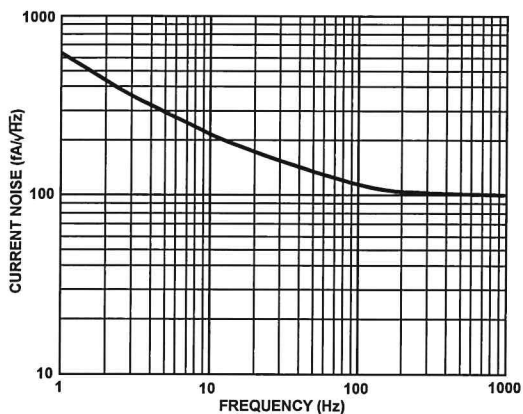


Figure 9. Current Noise Spectral Density vs. Frequency

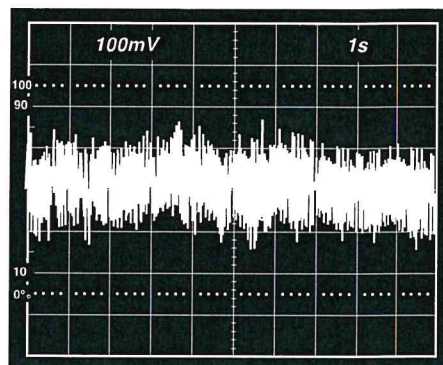


Figure 12. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div

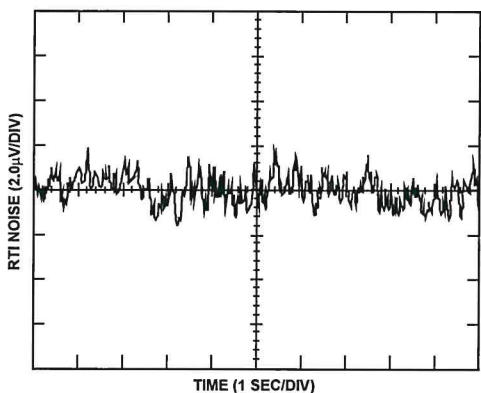


Figure 10. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

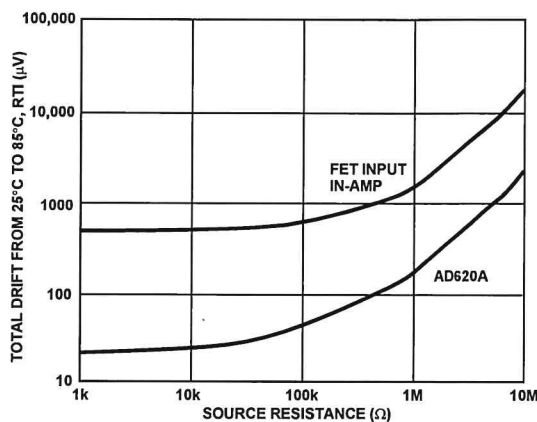


Figure 13. Total Drift vs. Source Resistance

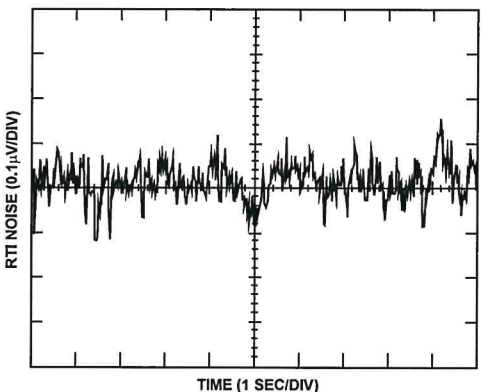


Figure 11. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

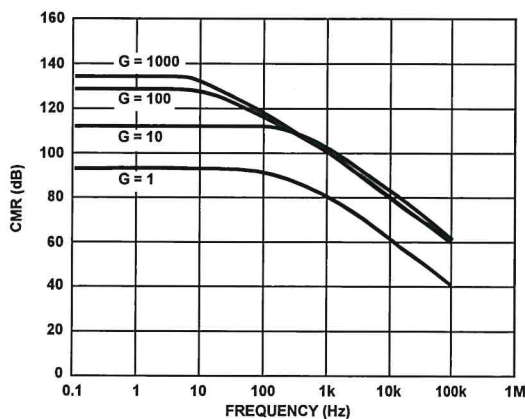


Figure 14. Typical CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance

AD620

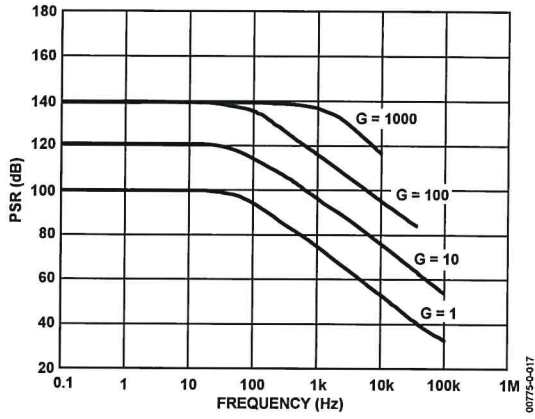


Figure 15. Positive PSR vs. Frequency, RTI (G = 1–1000)

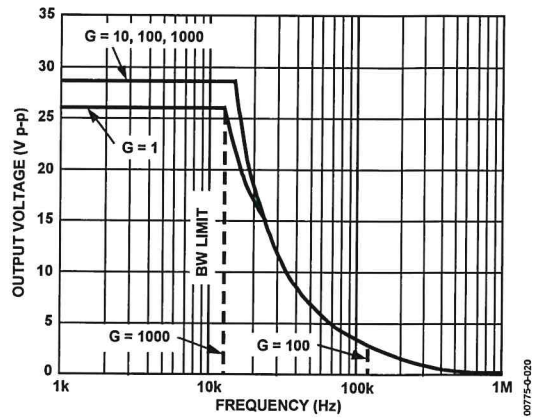


Figure 18. Large Signal Frequency Response

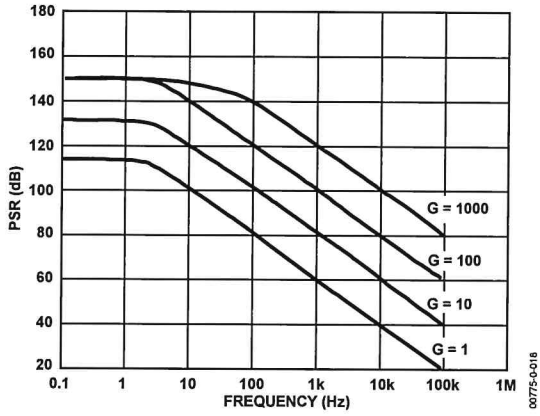


Figure 16. Negative PSR vs. Frequency, RTI (G = 1–1000)

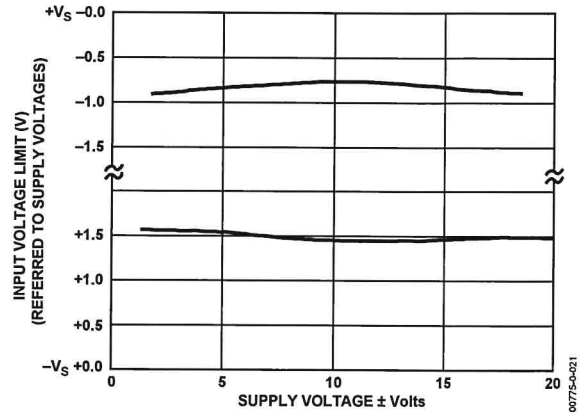


Figure 19. Input Voltage Range vs. Supply Voltage, G = 1

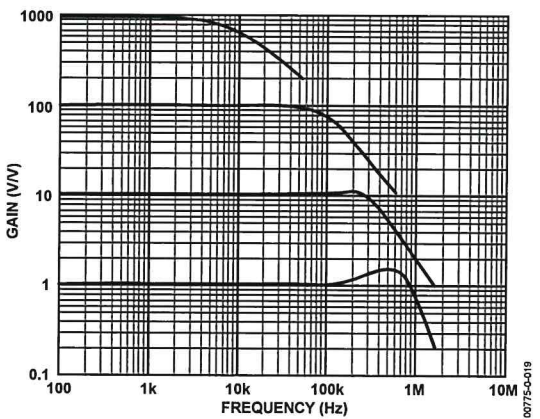


Figure 17. Gain vs. Frequency

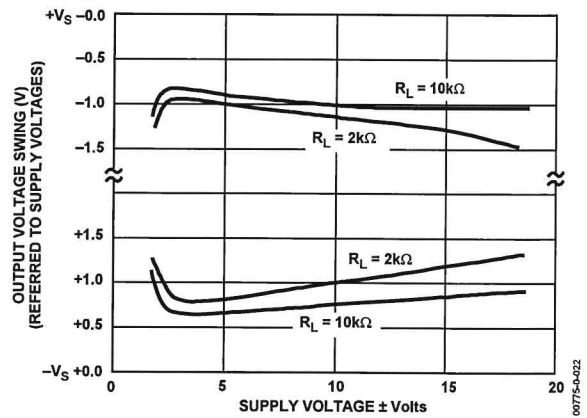


Figure 20. Output Voltage Swing vs. Supply Voltage, G = 10

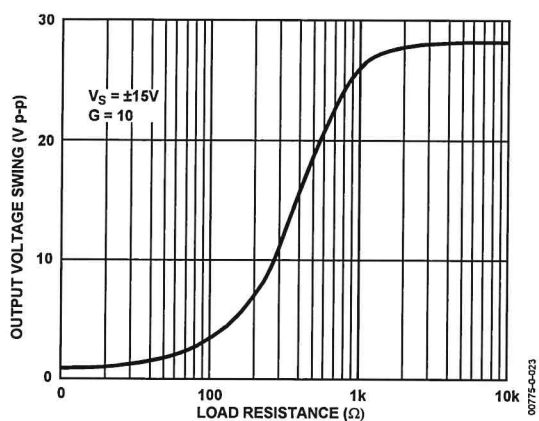


Figure 21. Output Voltage Swing vs. Load Resistance

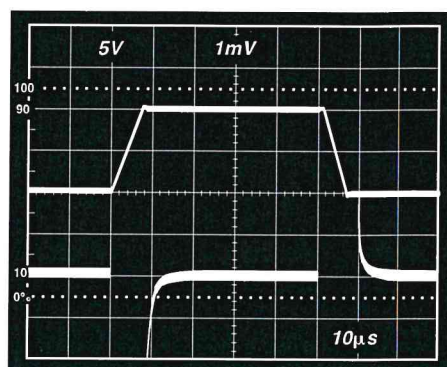


Figure 24. Large Signal Response and Settling Time, $G = 10$ ($0.5 \text{ mV} = 0.01\%$)

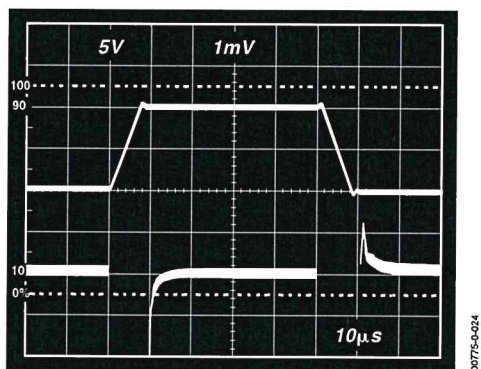


Figure 22. Large Signal Pulse Response and Settling Time $G = 1$ ($0.5 \text{ mV} = 0.01\%$)

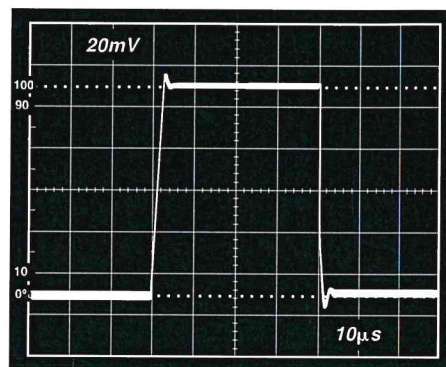


Figure 25. Small Signal Response, $G = 10$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$

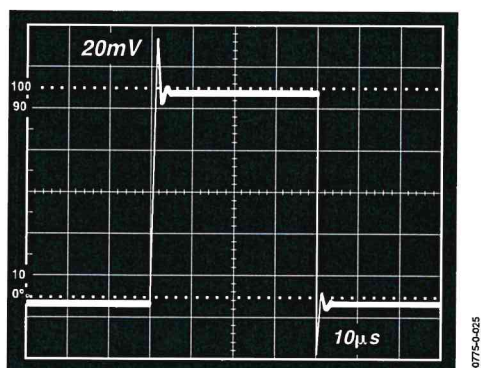


Figure 23. Small Signal Response, $G = 1$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$

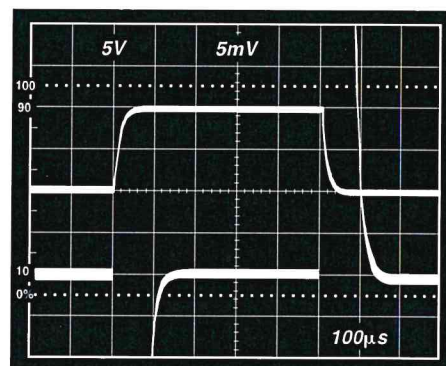


Figure 26. Large Signal Response and Settling Time, $G = 100$ ($0.5 \text{ mV} = 0.01\%$)

AD620

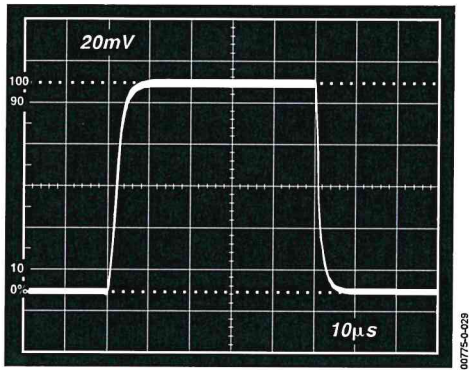


Figure 27. Small Signal Pulse Response, $G = 100$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$

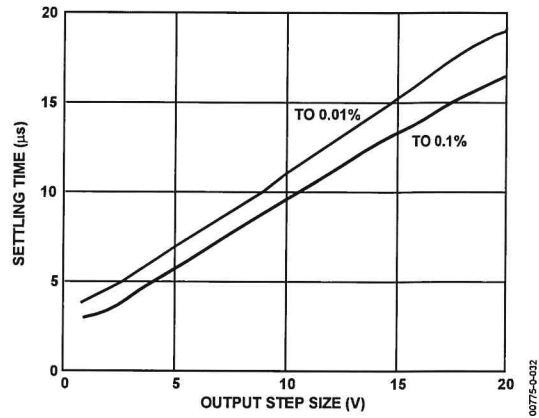


Figure 30. Settling Time vs. Step Size ($G = 1$)

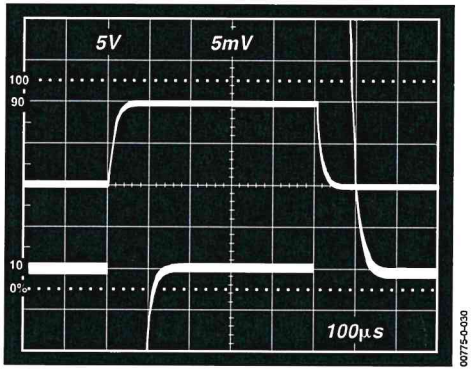


Figure 28. Large Signal Response and Settling Time, $G = 1000$ ($0.5 \text{ mV} = 0.01\%$)

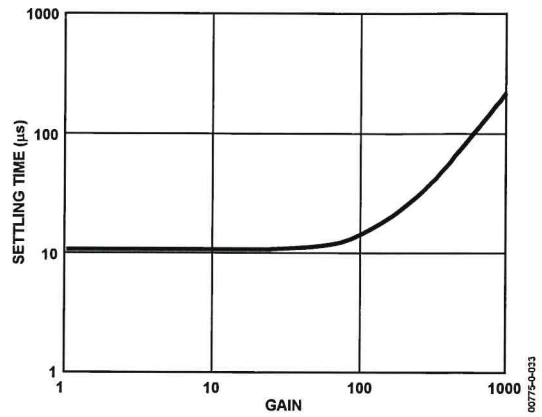


Figure 31. Settling Time to 0.01% vs. Gain, for a 10V Step

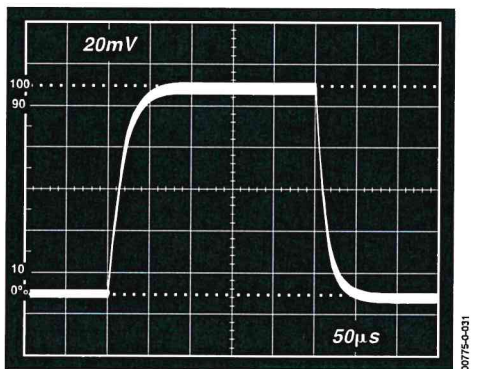


Figure 29. Small Signal Pulse Response, $G = 1000$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$

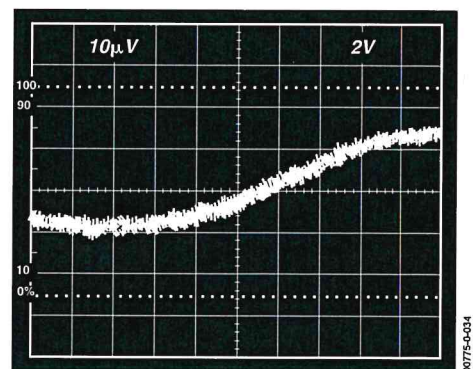


Figure 32. Gain Nonlinearity, $G = 1$, $R_L = 10 \text{ k}\Omega$ ($10 \text{ μV} = 1 \text{ ppm}$)

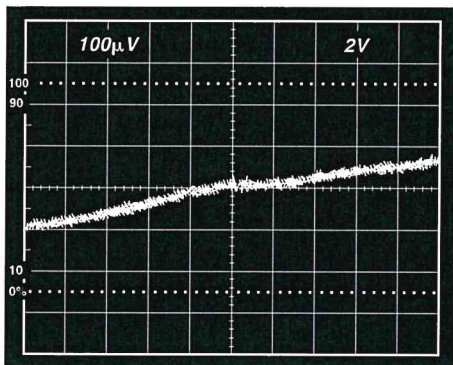


Figure 33. Gain Nonlinearity, $G = 100$, $R_L = 10\text{ k}\Omega$
($100\ \mu\text{V} = 10\text{ ppm}$)

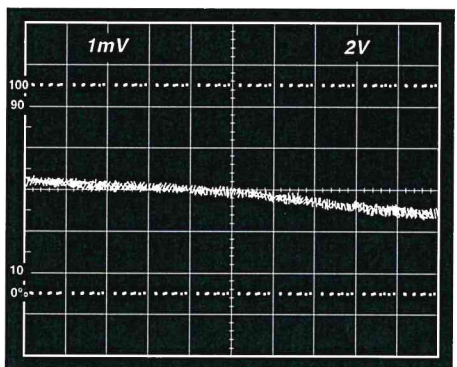


Figure 34. Gain Nonlinearity, $G = 1000$, $R_L = 10\text{ k}\Omega$
($1\text{ mV} = 100\text{ ppm}$)

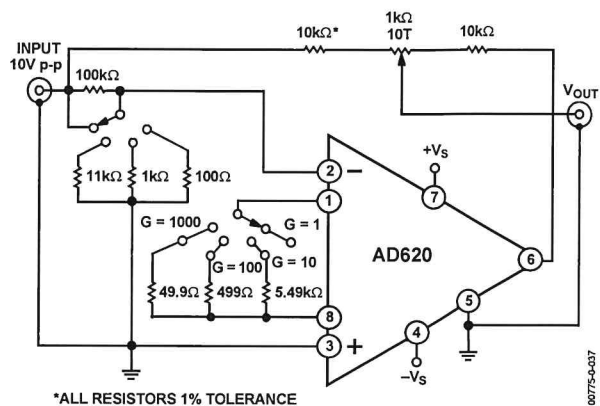


Figure 35. Settling Time Test Circuit

AD620

THEORY OF OPERATION

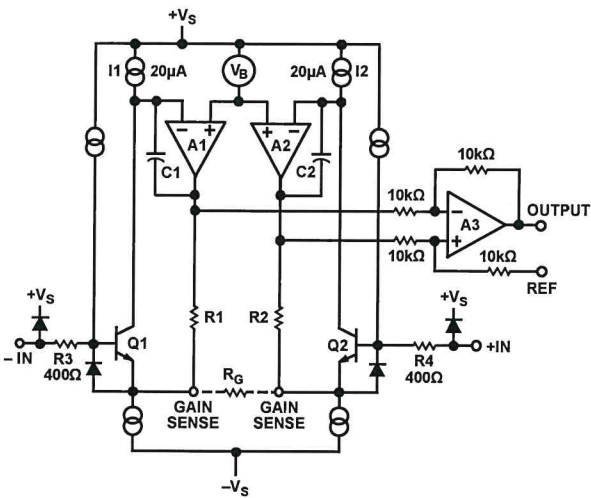


Figure 36. Simplified Schematic of AD620

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* (to 0.15% at $G = 100$) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 36), yet offer 10× lower input bias current thanks to Superbeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1 and Q2, thereby impressing the input voltage across the external gain setting resistor R_G . This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity-gain subtractor, A3, removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain related errors. (b) The gain-bandwidth product (determined by C1 and C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4k\Omega}{R_G} + 1$$

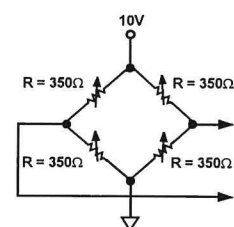
$$R_G = \frac{49.4k\Omega}{G-1}$$

Make vs. Buy: a Typical Bridge Application Error Budget

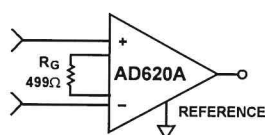
The AD620 offers improved performance over “homebrew” three op amp IA designs, along with smaller size, fewer components, and 10× lower supply current. In the typical application, shown in Figure 37, a gain of 100 is required to amplify a bridge output of 20 mV full-scale over the industrial temperature range of -40°C to +85°C. Table 4 shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system in which it is being used, the AD620 provides greater accuracy at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an autogain/autozero cycle removes all absolute accuracy and drift errors, leaving only the resolution errors of gain, nonlinearity, and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.



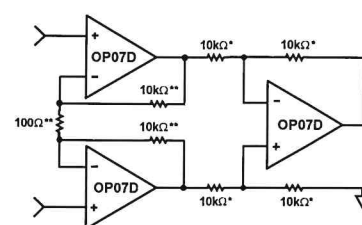
PRECISION BRIDGE TRANSDUCER



AD620A MONOLITHIC INSTRUMENTATION AMPLIFIER, G = 100

SUPPLY CURRENT = 1.3mA MAX

00775-04-00



"HOMEBREW" IN-AMP, G = 100
 *0.02% RESISTOR MATCH, 3ppm/°C TRACKING
 **DISCRETE 1% RESISTOR, 100ppm/°C TRACKING
 SUPPLY CURRENT = 15mA MAX

00775-04-01

Figure 37. Make vs. Buy

Table 4. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale	
			AD620	Homebrew
ABSOLUTE ACCURACY at $T_A = 25^\circ\text{C}$				
Input Offset Voltage, μV	125 $\mu\text{V}/20\text{ mV}$	$(150\ \mu\text{V} \times \sqrt{2})/20\text{ mV}$	6,250	10,607
Output Offset Voltage, μV	1000 $\mu\text{V}/100\text{ mV}/20\text{ mV}$	$((150\ \mu\text{V} \times 2)/100)/20\text{ mV}$	500	150
Input Offset Current, nA	2 nA $\times 350\ \Omega/20\text{ mV}$	$(6\text{ nA} \times 350\ \Omega)/20\text{ mV}$	18	53
CMR, dB	110 dB(3.16 ppm) $\times 5\text{ V}/20\text{ mV}$	$(0.02\% \text{ Match} \times 5\text{ V})/20\text{ mV}/100$	791	500
		Total Absolute Error	7,559	11,310
DRIFT TO 85°C				
Gain Drift, ppm/°C	$(50\text{ ppm} + 10\text{ ppm}) \times 60^\circ\text{C}$	100 ppm/°C Track $\times 60^\circ\text{C}$	3,600	6,000
Input Offset Voltage Drift, $\mu\text{V}/^\circ\text{C}$	1 $\mu\text{V}/^\circ\text{C} \times 60^\circ\text{C}/20\text{ mV}$	$(2.5\ \mu\text{V}/^\circ\text{C} \times \sqrt{2} \times 60^\circ\text{C})/20\text{ mV}$	3,000	10,607
Output Offset Voltage Drift, $\mu\text{V}/^\circ\text{C}$	15 $\mu\text{V}/^\circ\text{C} \times 60^\circ\text{C}/100\text{ mV}/20\text{ mV}$	$(2.5\ \mu\text{V}/^\circ\text{C} \times 2 \times 60^\circ\text{C})/100\text{ mV}/20\text{ mV}$	450	150
		Total Drift Error	7,050	16,757
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz to 10 Hz Voltage Noise, $\mu\text{V p-p}$	0.28 $\mu\text{V p-p}/20\text{ mV}$	$(0.38\ \mu\text{V p-p} \times \sqrt{2})/20\text{ mV}$	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,663	28,134

G = 100, $V_s = \pm 15\text{ V}$.

(All errors are min/max and referred to input.)

AD620

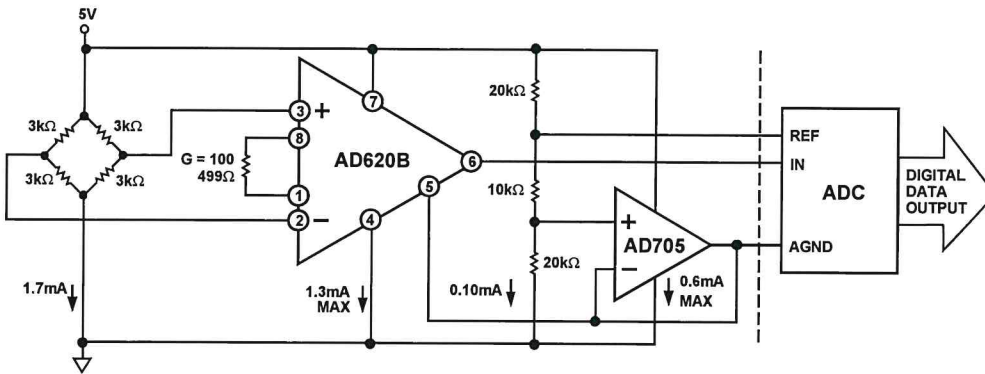


Figure 38. A Pressure Monitor Circuit that Operates on a 5 V Single Supply

Pressure Measurement

Although useful in many bridge applications, such as weigh scales, the AD620 is especially suitable for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 38 shows a 3 kΩ pressure transducer bridge powered from 5 V. In such a circuit, the bridge consumes only 1.7 mA. Adding the AD620 and a buffered voltage divider allows the signal to be conditioned for only 3.8 mA of total supply current.

Small size and low cost make the AD620 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it also serves applications such as diagnostic noninvasive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 39) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-lead mini-DIP and SOIC package offerings make it an excellent choice for battery-powered data recorders.

Furthermore, the low bias currents and low current noise, coupled with the low voltage noise of the AD620, improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

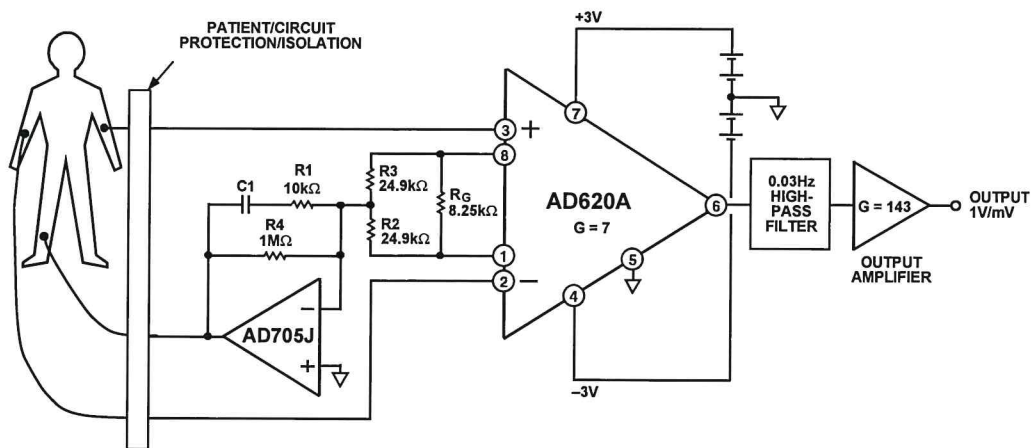


Figure 39. A Medical ECG Monitor Circuit

Precision V-I Converter

The AD620, along with another op amp and two resistors, makes a precision current source (Figure 40). The op amp buffers the reference terminal to maintain good CMR. The output voltage, V_x , of the AD620 appears across R_1 , which converts it to a current. This current, less only the input bias current of the op amp, then flows out to the load.

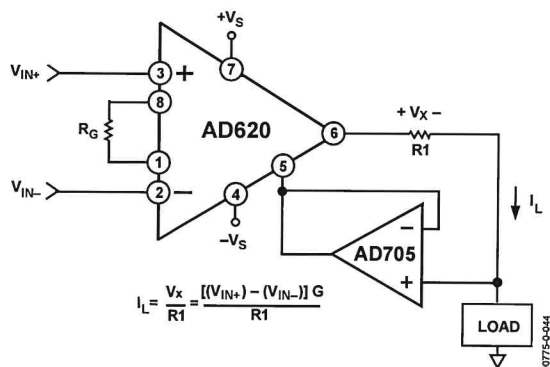


Figure 40. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

GAIN SELECTION

The AD620 gain is resistor-programmed by R_G , or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1% to 1% resistors. Table 5 shows required values of R_G for various gains. Note that for $G = 1$, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula:

$$R_G = \frac{49.4 \text{ k}\Omega}{G - 1}$$

To minimize gain error, avoid high parasitic resistance in series with R_G ; to minimize gain drift, R_G should have a low TC—less than 10 ppm/°C—for the best performance.

Table 5. Required Values of Gain Resistors

1% Std Table Value of $R_G(\Omega)$	Calculated Gain	0.1% Std Table Value of $R_G(\Omega)$	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003.0

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains, and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as

$$\text{Total Error RTI} = \text{input error} + (\text{output error}/G)$$

$$\text{Total Error RTO} = (\text{input error} \times G) + \text{output error}$$

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 safely withstands an input current of ±60 mA for several hours at room temperature. This is true for all gains and power on and off, which is useful if the signal source and amplifier are powered separately. For longer time periods, the input current should not exceed 6 mA.

For input voltages beyond the supplies, a protection resistor should be placed in series with each input to limit the current to 6 mA. These can be the same resistors as those used in the RFI filter. High values of resistance can impact the noise and AC CMRR performance of the system. Low leakage diodes (such as the BAV199) can be placed at the inputs to reduce the required protection resistance.

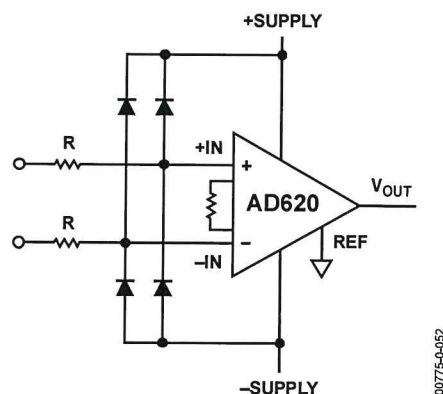


Figure 41. Diode Protection for Voltages Beyond Supply

RF INTERFERENCE

All instrumentation amplifiers rectify small out of band signals. The disturbance may appear as a small dc voltage offset. High frequency signals can be filtered with a low pass R-C network placed at the input of the instrumentation amplifier. Figure 42 demonstrates such a configuration. The filter limits the input

AD620

signal according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in $R \times C_C$ degrades the AD620 CMRR. To avoid inadvertently reducing CMRR-bandwidth performance, make sure that C_C is at least one magnitude smaller than C_D . The effect of mismatched C_C s is reduced with a larger $C_D:C_C$ ratio.

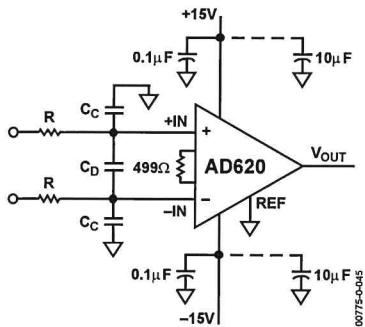


Figure 42. Circuit to Attenuate RF Interference

COMMON-MODE REJECTION

Instrumentation amplifiers, such as the AD620, offer high CMR, which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR, the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications, shielded cables are used to minimize noise; for best CMR over frequency, the shield should be properly driven. Figure 43 and Figure 44 show active data guards that are configured to improve ac common-mode rejections by “bootstrapping” the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

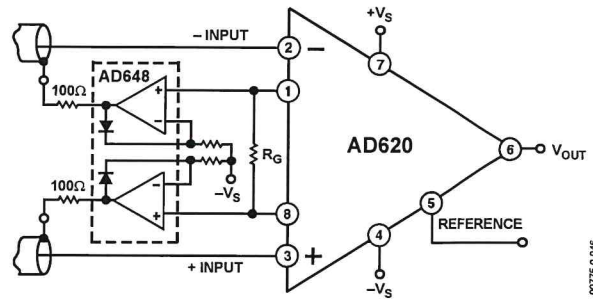


Figure 43. Differential Shield Driver

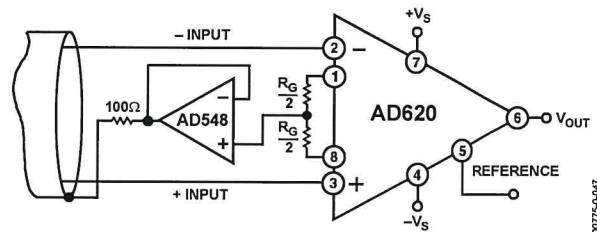


Figure 44. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate “local ground.”

To isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 45). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package shown in Figure 45.

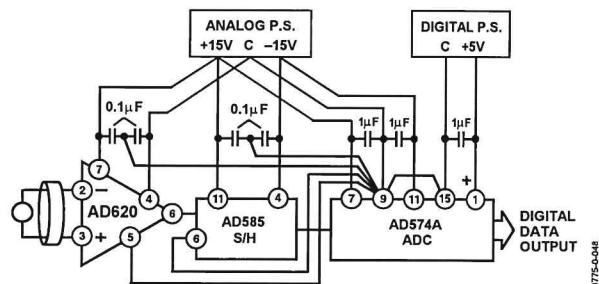


Figure 45. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents. Therefore, when amplifying “floating” input sources, such as transformers or ac-coupled sources, there must be a dc path from each input to ground, as shown in Figure 46, Figure 47, and Figure 48. Refer to *A Designer’s Guide to Instrumentation Amplifiers* (free from Analog Devices) for more information regarding in-amp applications.

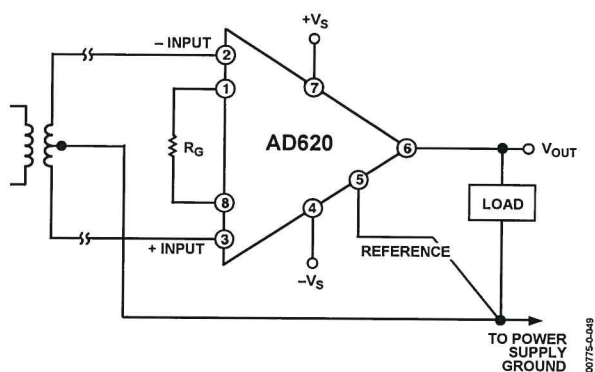


Figure 46. Ground Returns for Bias Currents with Transformer-Coupled Inputs

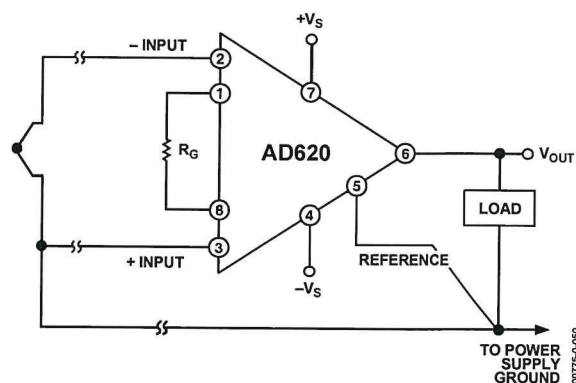


Figure 47. Ground Returns for Bias Currents with Thermocouple Inputs

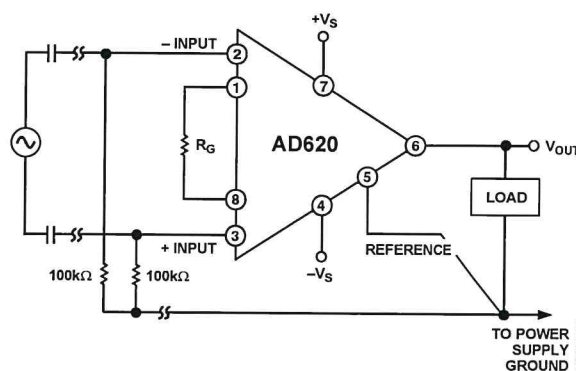


Figure 48. Ground Returns for Bias Currents with AC-Coupled Inputs

AD620

AD620ACHIPS INFORMATION

Die size: 1803 μm \times 3175 μm

Die thickness: 483 μm

Bond Pad Metal: 1% Copper Doped Aluminum

To minimize gain errors introduced by the bond wires, use Kelvin connections between the chip and the gain resistor, R_G , by connecting Pad 1A and Pad 1B in parallel to one end of R_G and Pad 8A and Pad 8B in parallel to the other end of R_G . For unity gain applications where R_G is not required, Pad 1A and Pad 1B must be bonded together as well as the Pad 8A and Pad 8B.

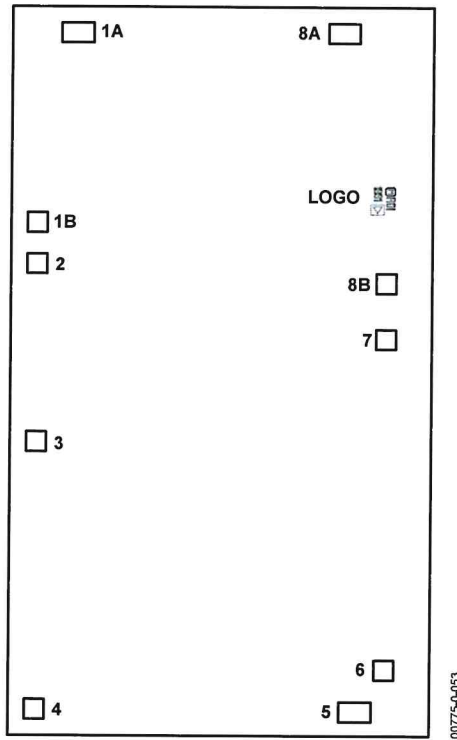


Figure 49. Bond Pad Diagram

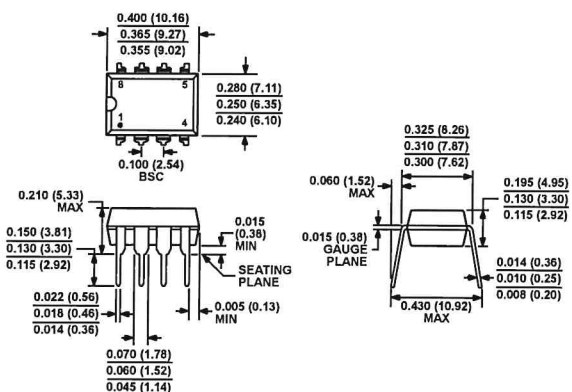
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Table 6. Bond Pad Information

Pad No.	Mnemonic	Pad Coordinates ¹	
		X (μm)	Y (μm)
1A	R_G	-623	+1424
1B	R_G	-789	+628
2	-IN	-790	+453
3	+IN	-790	-294
4	$-V_S$	-788	-1419
5	REF	+570	-1429
6	OUTPUT	+693	-1254
7	$+V_S$	+693	+139
8A	R_G	+505	+1423
8B	R_G	+693	+372

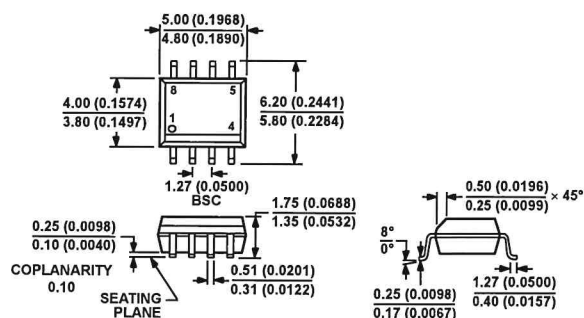
¹ The pad coordinates indicate the center of each pad, referenced to the center of the die. The die orientation is indicated by the logo, as shown in Figure 49.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

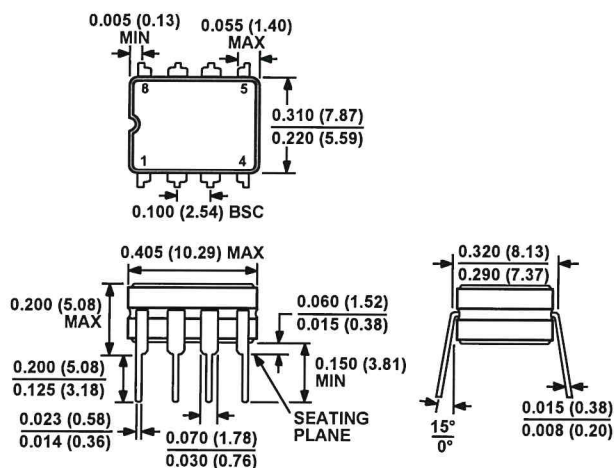
Figure 50. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8).
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 52. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8).
Dimensions shown in millimeters and (inches)

012407-A



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

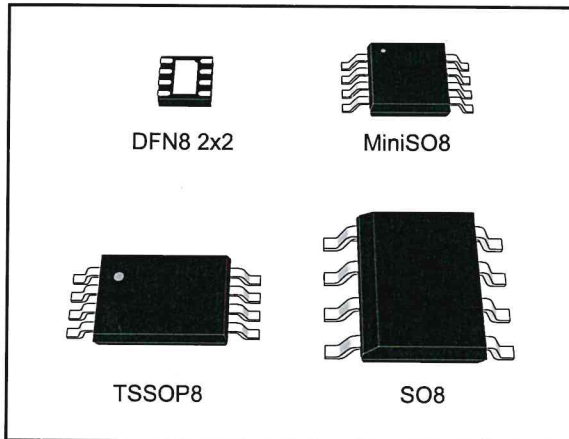
Figure 51. 8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8).
Dimensions shown in inches and (millimeters)

AD620

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD620AN	-40°C to +85°C	8-Lead PDIP	N-8
AD620ANZ	-40°C to +85°C	8-Lead PDIP	N-8
AD620BN	-40°C to +85°C	8-Lead PDIP	N-8
AD620BNZ	-40°C to +85°C	8-Lead PDIP	N-8
AD620AR	-40°C to +85°C	8-Lead SOIC_N	R-8
AD620ARZ	-40°C to +85°C	8-Lead SOIC_N	R-8
AD620AR-REEL	-40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD620ARZ-REEL	-40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD620AR-REEL7	-40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD620ARZ-REEL7	-40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD620BR	-40°C to +85°C	8-Lead SOIC_N	R-8
AD620BRZ	-40°C to +85°C	8-Lead SOIC_N	R-8
AD620BR-REEL	-40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD620BRZ-RL	-40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD620BR-REEL7	-40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD620BRZ-R7	-40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD620ACHIPS	-40°C to +85°C	Die Form	
AD620SQ/883B	-55°C to +125°C	8-Lead CERDIP	Q-8

¹ Z = RoHS Compliant Part.



Features

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current per channel essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing
0 V to ($V_{CC+} - 1.5$ V)

Related products

- See LM158W for enhanced ESD ratings
- See LM2904 and LM2904W for automotive grade versions

Description

These circuits consist of two independent, high-gain, internally frequency-compensated op amps, specifically designed to operate from a single power supply over a wide range of voltages. The low-power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard 5 V, which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

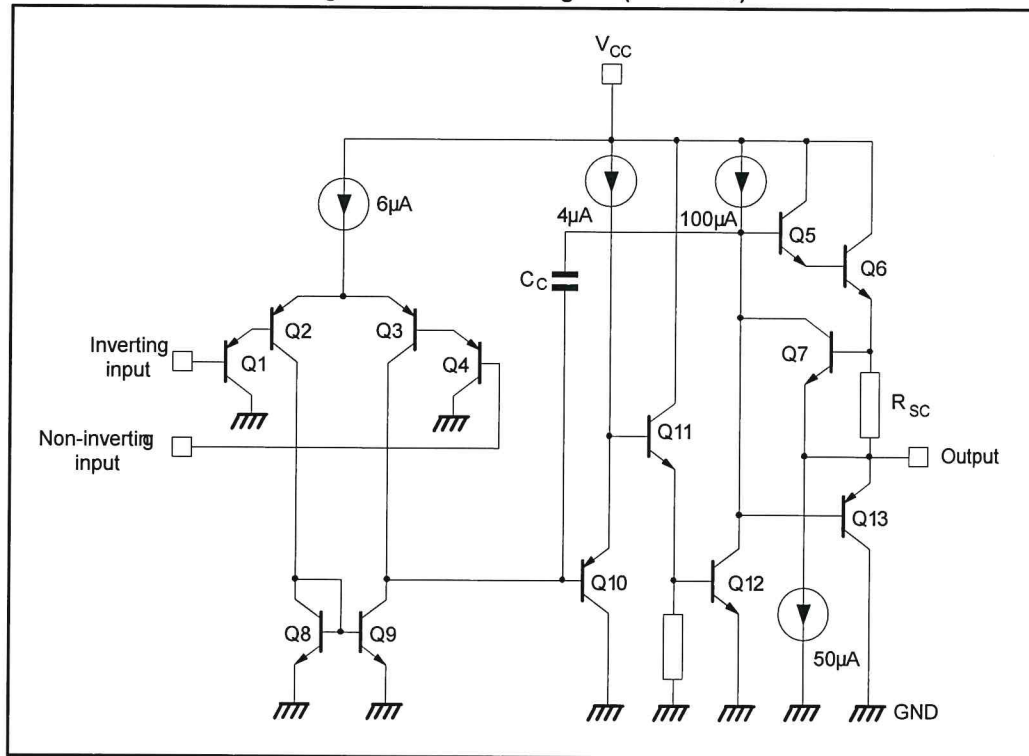
In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

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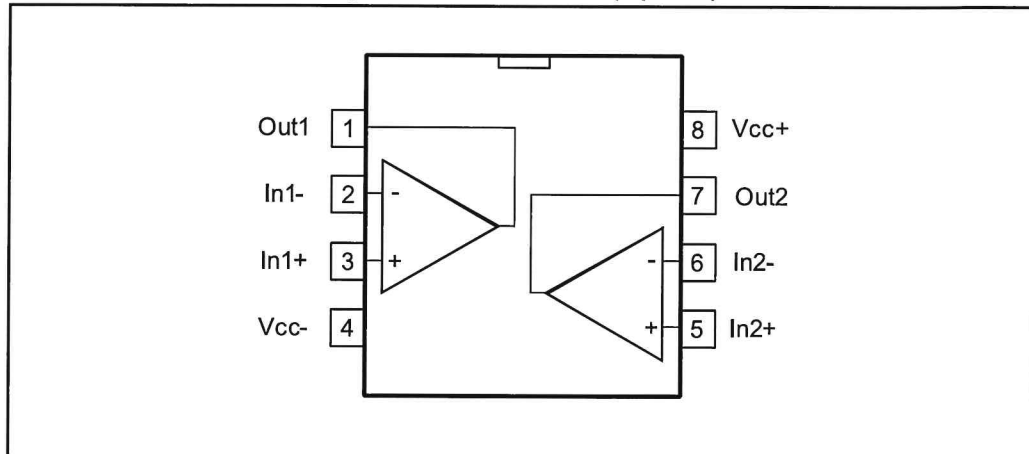
1 Schematic diagram

Figure 1: Schematic diagram (1/2 LM158)



2 Package pin connections

Figure 2: Pin connections (top view)



1. The exposed pad of the DFN8 2x2 can be left floating or connected to ground

3 Absolute maximum ratings

Table 1: Absolute maximum ratings

Symbol	Parameter	LM158,A	LM258,A	LM358,A	Unit
V _{CC}	Supply voltage	±16 or 32			V
V _i	Input voltage	-0.3 to 32			
V _{id}	Differential input voltage	±32			
	Output short-circuit duration ⁽¹⁾	Infinite			
I _{in}	Input current ⁽²⁾	5 mA in DC or 50 mA in AC (duty cycle = 10 %, T = 1 s)			mA
T _{oper}	Operating free-air temperature range	-55 to 125	-40 to 105	0 to 70	°C
T _{stg}	Storage temperature range	-65 to 150			
T _j	Maximum junction temperature	150			
R _{thja}	Thermal resistance junction to ambient ⁽³⁾	SO8	125		°C/W
		MiniSO8	190		
		DFN8 2x2	57		
		TSSOP8	120		
R _{thjc}	Thermal resistance junction to case ⁽³⁾	SO8	40		
		MiniSO8	39		
		TSSOP8	37		
ESD	HBM: human body model ⁽⁴⁾	300			V
	MM: machine model ⁽⁵⁾	200			
	CDM: charged device model ⁽⁶⁾	1.5			kV

Notes:

⁽¹⁾Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15 V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short circuits on all amplifiers.

⁽²⁾This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.

⁽³⁾Short-circuits can cause excessive heating and destructive dissipation. R_{th} are typical values.

⁽⁴⁾Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

⁽⁵⁾Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

⁽⁶⁾Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Absolute maximum ratings

LM158, LM258, LM358, LM158A, LM258A, LM358A

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	3 to 30	V
V _{icm}	Common mode input voltage range T _{amb} = 25°C ⁽¹⁾	(V _{CC-}) to (V _{CC+} - 1.5)	
	Common mode input voltage range (T _{min} ≤ T _{amb} ≤ T _{max}) ⁽²⁾	(V _{CC-}) to (V _{CC+} - 2)	
T _{oper}	Operating free air temperature range	LM158	-55 to 125
		LM258	-40 to 105
		LM358	0 to 70
			°C

Notes:

⁽¹⁾When used in comparator, the functionality is guaranteed as long as at least one input remains within the operating common mode voltage range.

⁽²⁾When used in comparator, the functionality is guaranteed as long as at least one input remains within the operating common mode voltage range.

4 Electrical characteristics

Table 3: Electrical characteristics for $V_{CC+} = 5\text{ V}$, $V_{CC-} = \text{Ground}$, $V_o = 1.4\text{ V}$, $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$
(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	
V_{io}	Input offset voltage ⁽¹⁾	LM158A		2	mV	
		LM258A, LM358A	1	3		
		LM158, LM258		5		
		LM358	2	7		
	$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	LM158A, LM258A, LM358A		4		
		LM158, LM258		7		
LM358			9			
$\Delta V_{io}/\Delta T$	Input offset voltage drift	LM158A, LM258A, LM358A	7	15	$\mu\text{V}/^{\circ}\text{C}$	
		LM158, LM258, LM358	7	30		
I_{io}	Input offset current	LM158A, LM258A, LM358A	2	10	nA	
		LM158, LM258, LM358	2	30		
	$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	LM158A, LM258A, LM358A		30		
		LM158, LM258, LM358		40		
$\Delta I_{io}/\Delta T$	Input offset current drift	LM158A, LM258A, LM358A	10	200	$\text{pA}/^{\circ}\text{C}$	
		LM158, LM258, LM358	10	300		
I_{ib}	Input bias current ⁽²⁾	LM158A, LM258A, LM358A	20	50	nA	
		LM158, LM258, LM358	20	150		
	$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	LM158A, LM258A, LM358A		100		
		LM158, LM258, LM358		200		
A_{vd}	Large signal voltage gain	$V_{CC+} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_o = 1.4\text{ V to } 11.4\text{ V}$	50	100	V/mV	
		$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	25			
SVR	Supply voltage rejection ratio	$V_{CC+} = 5\text{ V to } 30\text{ V}$, $R_s \leq 10\text{ k}\Omega$	65	100	dB	
		$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	65			
I_{CC}	Supply current, all amp, no load	$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$ $V_{CC+} = 5\text{ V}$	0.7	1.2	mA	
		$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$ $V_{CC+} = 30\text{ V}$		2		
CMR	Common mode rejection ratio	$R_s \leq 10\text{ k}\Omega$	70	85	dB	
		$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	60			
I_{source}	Output current source	$V_{CC+} = 15\text{ V}$, $V_o = 2\text{ V}$, $V_{id} = 1\text{ V}$	20	40	60	mA
I_{sink}	Output sink current	$V_{CC+} = 15\text{ V}$, $V_o = 2\text{ V}$, $V_{id} = -1\text{ V}$	10	20		mA
		$V_{CC+} = 15\text{ V}$, $V_o = 0.2\text{ V}$, $V_{id} = -1\text{ V}$	12	50		μA

Electrical characteristics

LM158, LM258, LM358, LM158A, LM258A, LM358A

Symbol	Parameter	Min.	Typ.	Max.	Unit	
V _{OH}	High level output voltage	V _{CC+} = 30 V, R _L = 2 kΩ connected to V _{CC-} , T _{amb} = 25 °C	26	27		V
		V _{CC+} = 30 V, R _L = 2 kΩ connected to V _{CC-} , T _{min} ≤ T _{amb} ≤ T _{max}	26			
		V _{CC+} = 30 V, R _L = 10 kΩ connected to V _{CC-} , T _{amb} = 25 °C	27	28		
		V _{CC+} = 30 V, R _L = 10 kΩ connected to V _{CC-} , T _{min} ≤ T _{amb} ≤ T _{max}	27			
		V _{CC+} = 5 V, R _L = 2 kΩ connected to V _{CC-} , T _{amb} = 25 °C	3.5			
		V _{CC+} = 5 V, R _L = 2 kΩ connected to V _{CC-} , T _{min} ≤ T _{amb} ≤ T _{max}	3			
V _{OL}	Low level output voltage	R _L = 10 kΩ connected to V _{CC-}		5	20	mV
		T _{min} ≤ T _{amb} ≤ T _{max}			20	
SR	Slew rate	V _{CC+} = 15 V, V _i = 0.5 to 3 V, R _L = 2 kΩ, C _L = 100 pF, unity gain	0.3	0.6		V/μs
GBP	Gain bandwidth product	V _{CC+} = 30 V, f = 100 kHz, V _{in} = 10 mV, R _L = 2 kΩ, C _L = 100 pF	0.7	1.1		MHz
THD	Total harmonic distortion	f = 1 kHz, A _v = 20 dB, R _L = 2 kΩ, V _o = 2 V _{pp} , C _L = 100 pF, V _o = 2 V _{pp}		0.02		%
e _n	Equivalent input noise voltage	f = 1 kHz, R _s = 100 Ω, V _{CC+} = 30 V		55		$\frac{nV}{\sqrt{Hz}}$
V _{o1} /V _{o2}	Channel separation ⁽³⁾	1 kHz ≤ f ≤ 20 kHz		120		dB

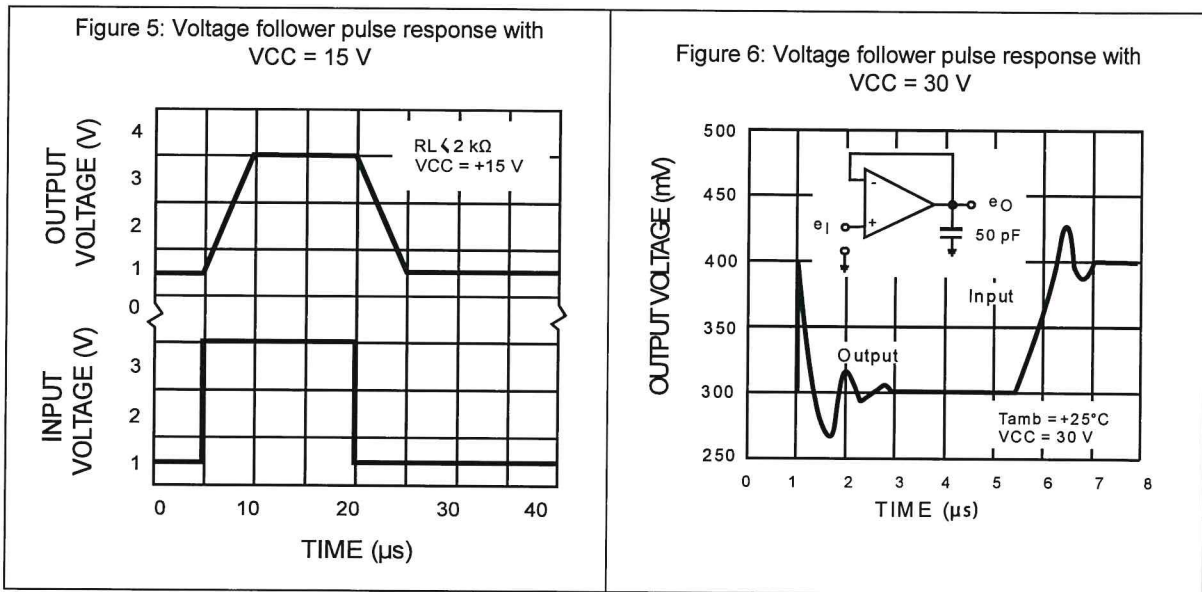
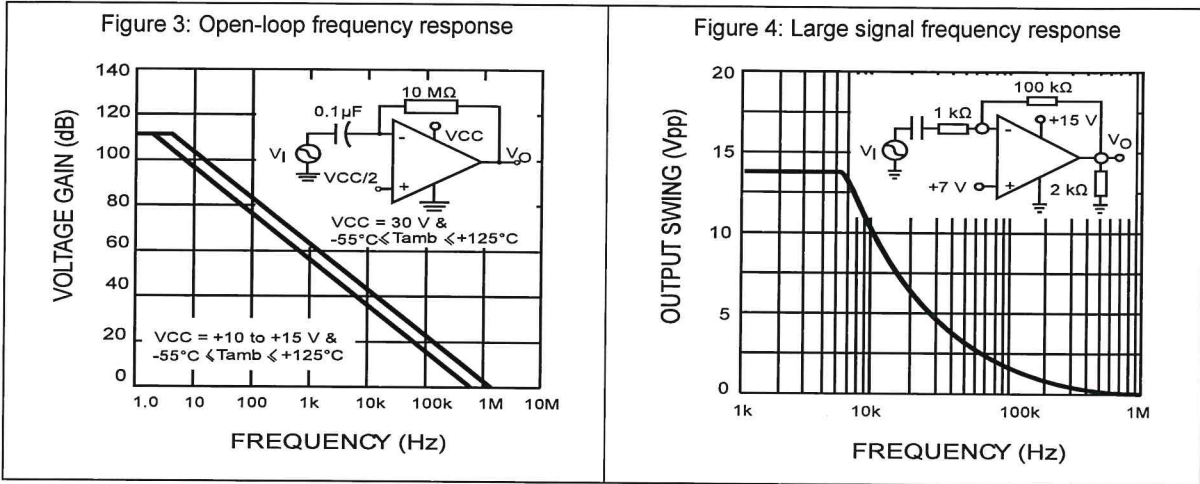
Notes:

⁽¹⁾V_O = 1.4 V, R_s = 0 Ω, 5 V < V_{CC+} < 30 V, 0 < V_{ic} < V_{CC+} - 1.5 V

⁽²⁾The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.

⁽³⁾Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

5 Electrical characteristic curves



Electrical characteristic curves

LM158, LM258, LM358, LM158A, LM258A, LM358A

Figure 7: Input current

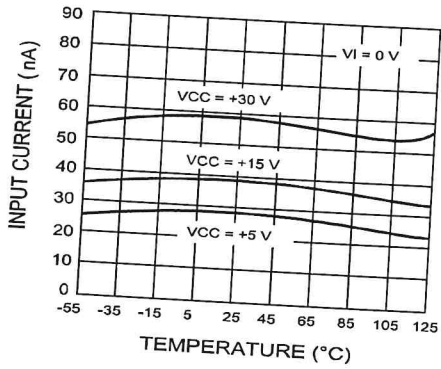


Figure 8: Output voltage vs sink current

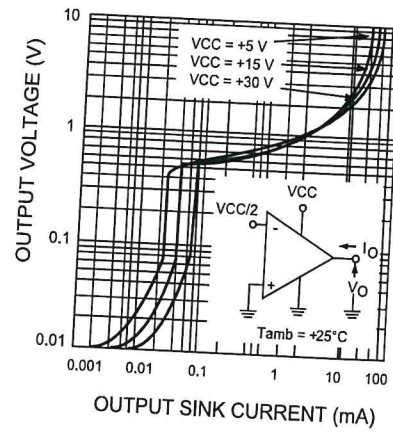


Figure 9: Output voltage vs source current

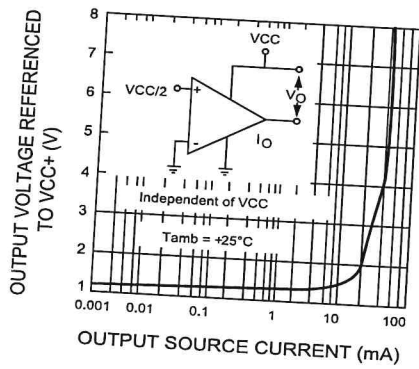


Figure 10: Current limiting

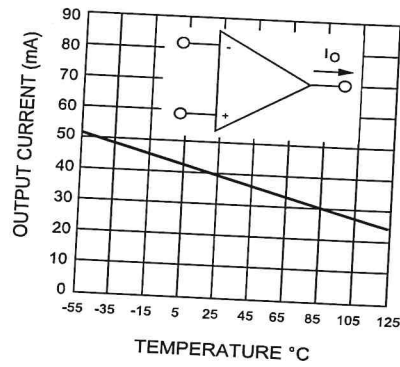


Figure 11: Input voltage range

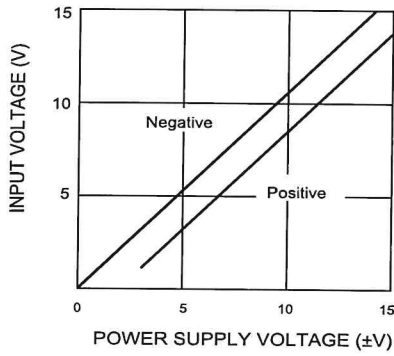


Figure 12: Open-loop gain

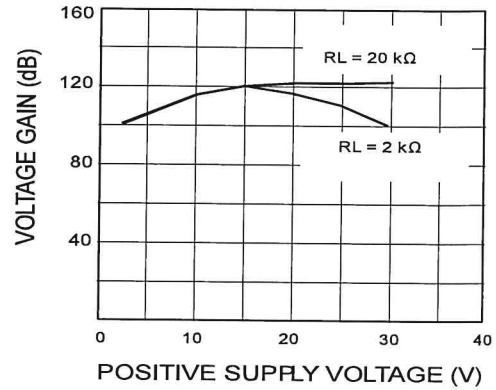


Figure 13: Supply current

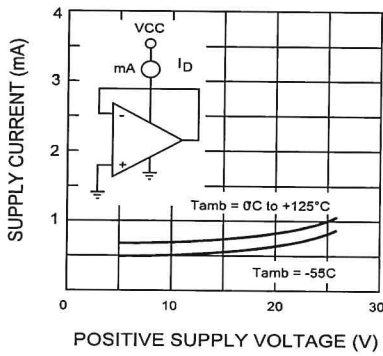


Figure 14: Input current

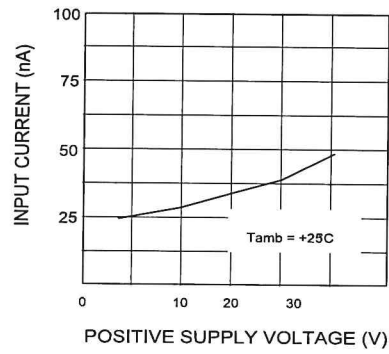


Figure 15: Gain bandwidth product

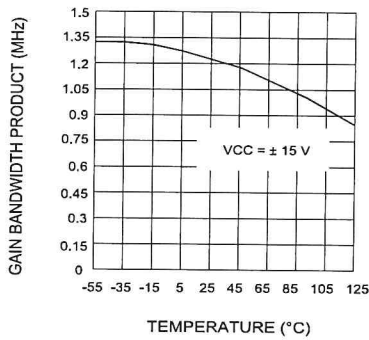
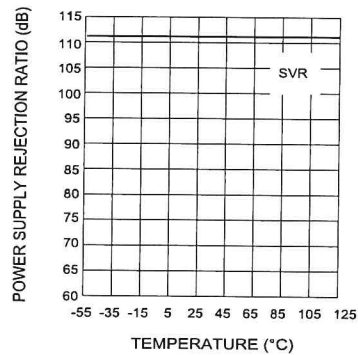


Figure 16: Power supply rejection ratio



Electrical characteristic curves

LM158, LM258, LM358, LM158A, LM258A, LM358A

Figure 17: Common-mode rejection ratio

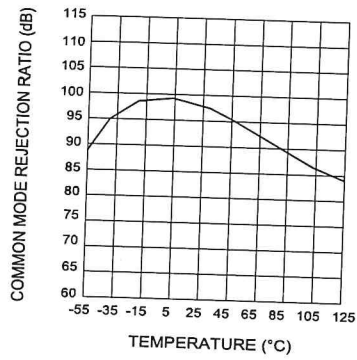
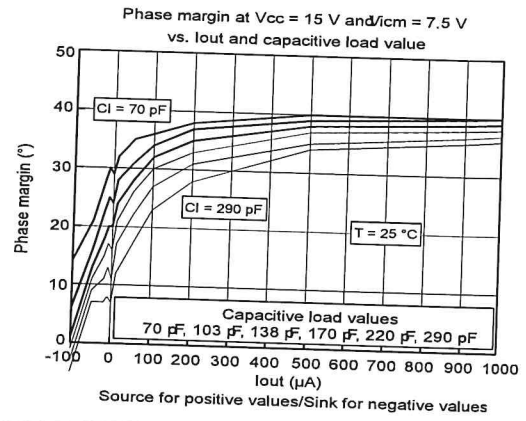


Figure 18: Phase margin vs. capacitive load



6 Typical applications

Single supply voltage $V_{CC} = 5 V_{DC}$.

Figure 19: AC-coupled inverting amplifier

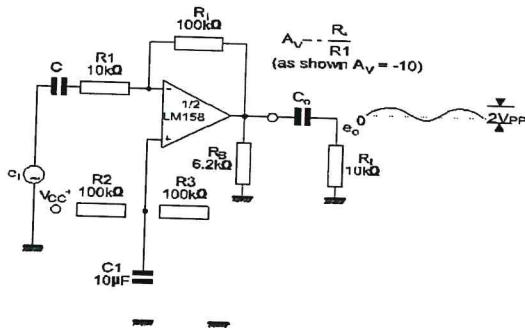


Figure 20: Non-inverting DC amplifier

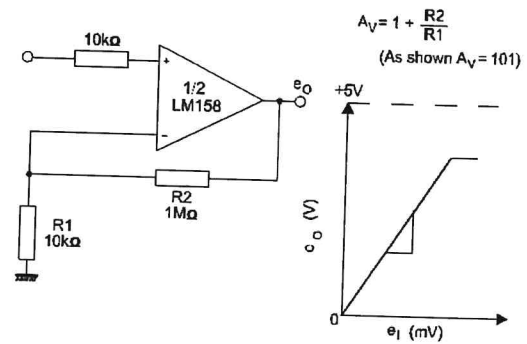


Figure 21: AC-coupled non-inverting amplifier

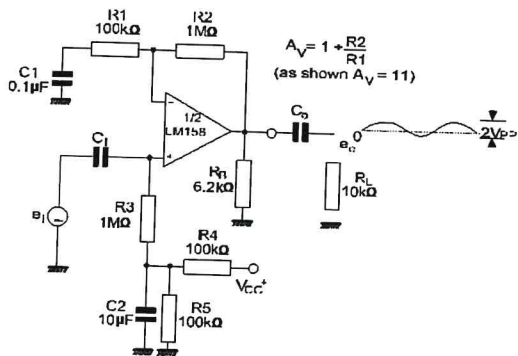
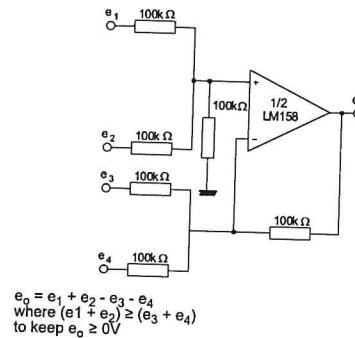


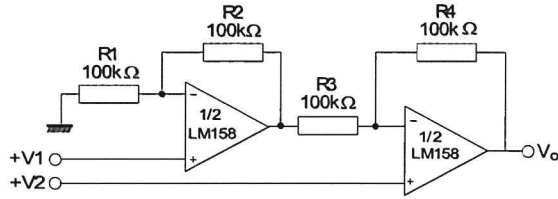
Figure 22: DC summing amplifier



Typical applications

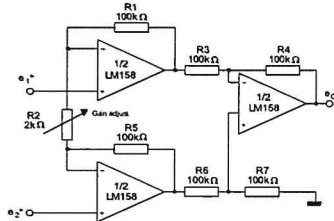
LM158, LM258, LM358, LM158A, LM258A, LM358A

Figure 23: High input Z, DC differential amplifier



if $R1 = R5$ and $R3 = R4 = R6 = R7$
 $e_o = [1 + \frac{2R1}{R2}] (e_2 + e_1)$
 As shown $e_o = 101 (e_2 + e_1)$

Figure 24: High input Z adjustable gain DC instrumentation amplifier



if $R1 = R5$ and
 $R3 = R4 = R6 = R7$
 $e_o = [1 + \frac{2R1}{R2}] (e_2 + e_1)$

As shown $e_o = 101 (e_2 + e_1)$

Figure 25: Using symmetrical amplifiers to reduce input current

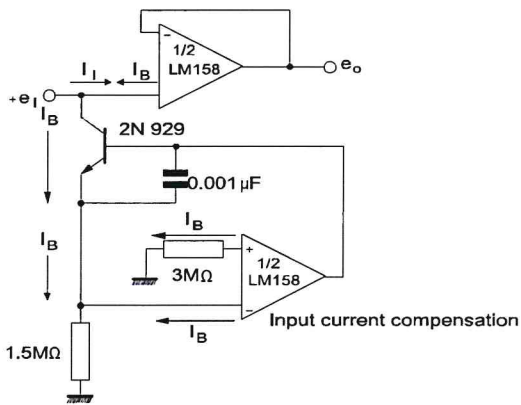


Figure 26: Low drift peak detector

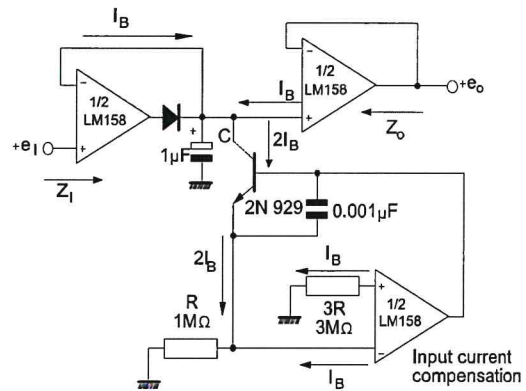
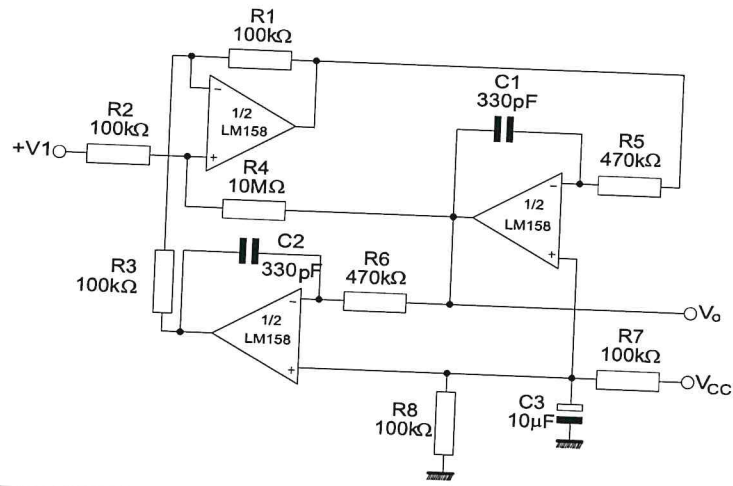


Figure 27: Active band-pass filter



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 SO8 package information

Figure 28: SO8 package outline

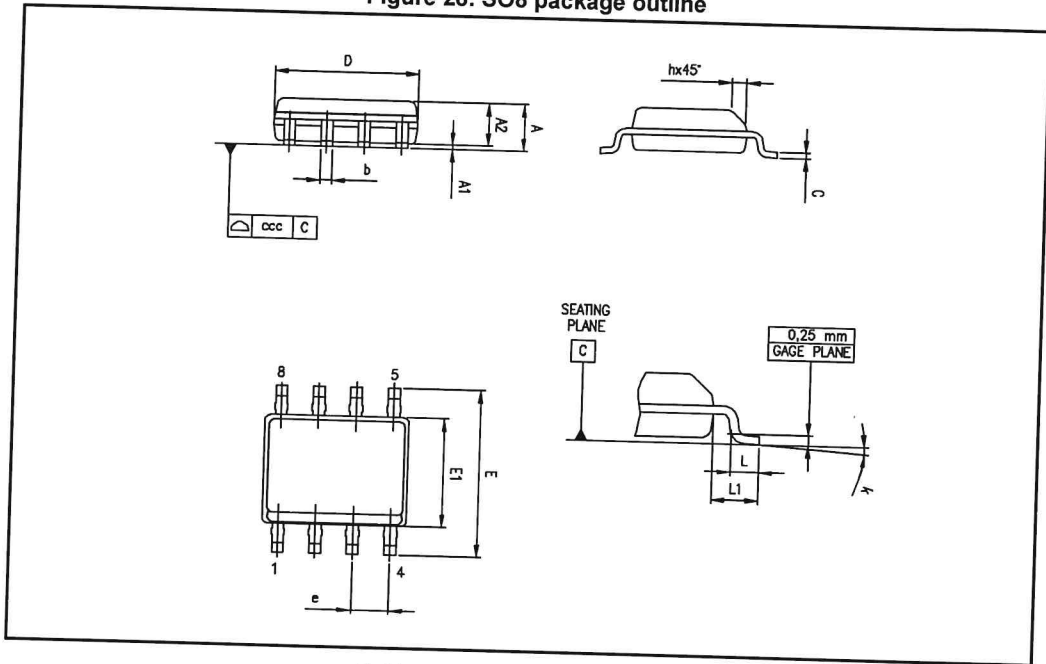


Table 4: SO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

7.2 MiniSO8 package information

Figure 29: MiniSO8 package outline

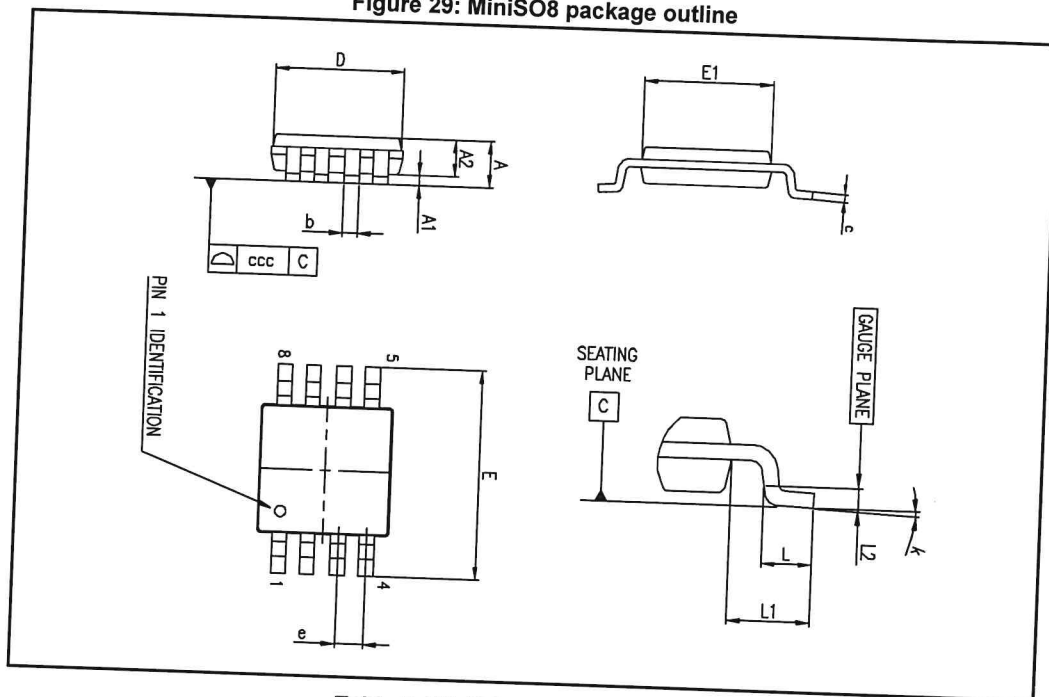


Table 5: MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

7.3 DFN8 2x2 package information

Figure 30: DFN8 2x2 package outline

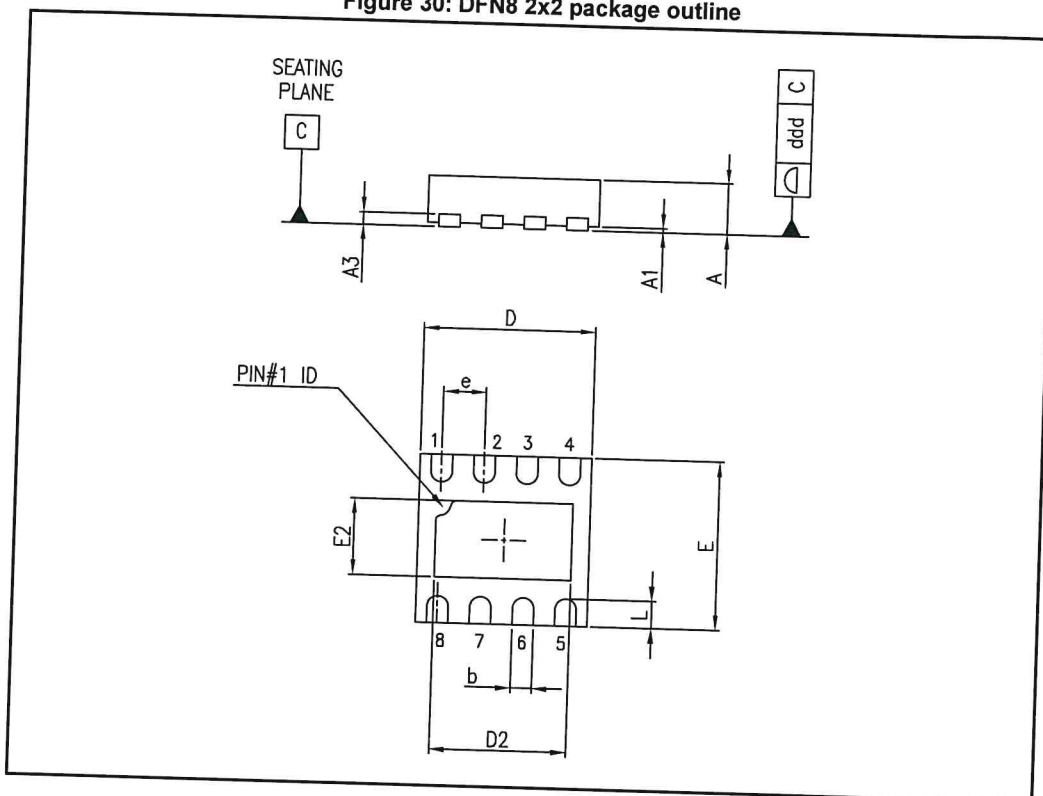
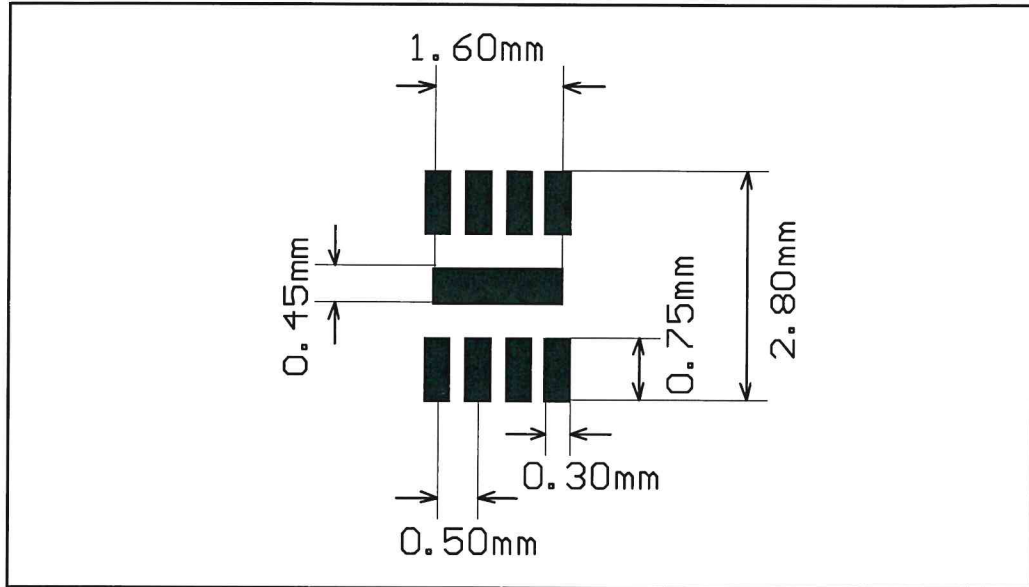


Table 6: DFN8 2x2 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L		0.3	0.425		0.012	0.017
ddd			0.08			0.003

Figure 31: DFN8 2x2 recommended footprint



7.4 TSSOP8 package information

Figure 32: TSSOP8 package outline

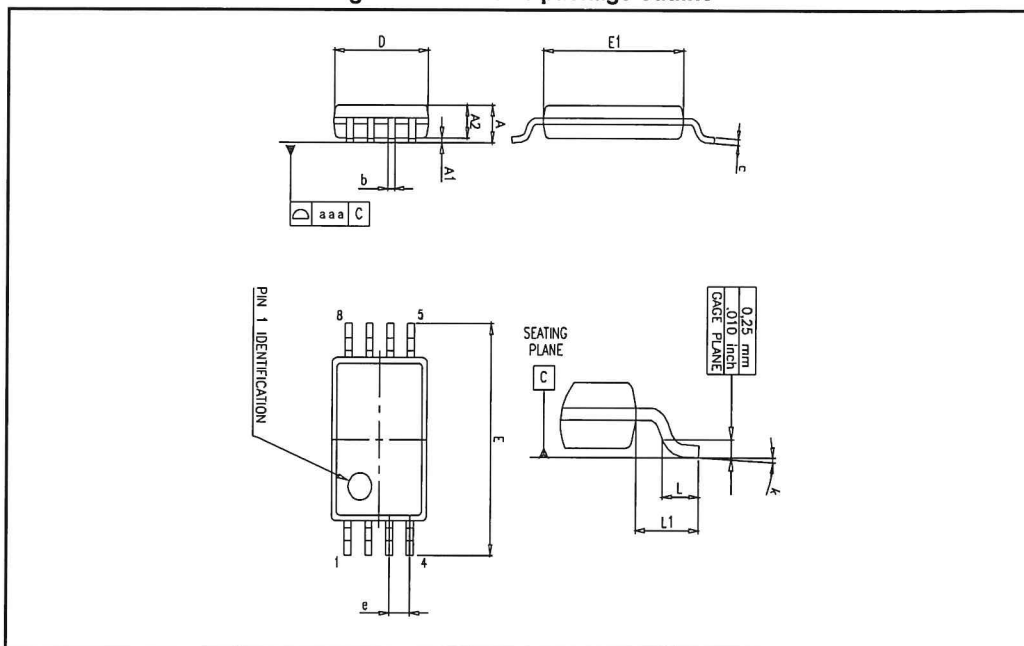


Table 7: TSSOP8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	

8 Ordering information

Table 8: Order codes

Order code	Temperature range	Package	Packaging	Marking
LM158QT	-55 °C to 125 °C	DFN8 2x2	Tape and reel	K4A
LM158DT		SO8		158
LM258ADT	-40 °C to 105 °C	SO8		258A
LM258AYDT ⁽¹⁾		SO8, automotive grade		258AY
LM258DT		SO8		258
LM258APT		TSSOP8		258A
LM258AST		MiniSO8		K408
LM258QT		DFN8 2x2		K4C
LM358DT		0 °C to 70 °C		SO8
LM358YDT ⁽¹⁾	SO8, automotive grade			358Y
LM358ADT	SO8			358A
LM358PT	TSSOP8			358
LM358APT				358A
LM358ST	MiniSO8			K405
LM358AST				K404
LM358QT	DFN8 2x2			K4E

Notes:

⁽¹⁾Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

9 Revision history

Table 9: Document revision history

Date	Revision	Changes
01-Jul-2003	1	First release.
02-Jan-2005	2	R_{thja} and T_j parameters added in AMR Table 1: "Absolute maximum ratings".
01-Jul-2005	3	ESD protection inserted in Table 1: "Absolute maximum ratings".
05-Oct-2006	4	Added Figure 17: Phase margin vs. capacitive load.
30-Nov-2006	5	Added missing ordering information.
25-Apr-2007	6	Removed LM158A, LM258A and LM358A from document title. Corrected error in MiniSO-8 package data. L1 is 0.004 inch. Added automotive grade order codes in Section 7: "Ordering information".
12-Feb-2008	7	Corrected V_{CC} max (30 V instead of 32 V) in operating conditions. Changed presentation of electrical characteristics table. Deleted V_{opp} parameter in electrical characteristics table. Corrected miniSO-8 package information. Corrected temperature range for automotive grade order codes. Updated automotive grade footnotes in order codes table.
26-Aug-2008	8	Added limitations on input current in Table 1: "Absolute maximum ratings". Corrected title for Figure 11. Added E and L1 parameters in Table 4: "SO8 package mechanical data". Changed Figure 31: "TSSOP8 package mechanical drawing".
02-Sep-2011	9	In Section 6: "Package information", added: <ul style="list-style-type: none"> • DFN8 2 x 2 mm package mechanical drawing • DFN8 2 x 2 mm recommended footprint • DFN8 2 x 2 mm order codes.
06-Apr-2012	10	Removed order codes LM158YD, LM258AYD, LM258YD and LM358YD from Table 8: "Order codes".
11-Jun-2013	11	Table 8: "Order codes": removed order codes LM158D, LM158YDT, LM258YDT, and LM258AD; added automotive grade qualification to order codes LM258ATDT and LM358YDT; updated marking for order codes LM158DT and LM258D/LM258DT; updated temperature range, packages, and packaging for several order codes.

Revision history

LM158, LM258, LM358, LM158A, LM258A,
LM358A

Date	Revision	Changes
20-Jun-2014	12	<p>Removed DIP8 package</p> <p>Corrected typos (W replaced with Ω, £ replaced with \leq)</p> <p>Updated Features</p> <p>Added Related products</p> <p>Table 3: replaced DV_{io} with $\Delta V_{io}/\Delta T$ and DI_{io} with $\Delta I_{io}/\Delta T$.</p> <p>Updated Table 7 for exposed pad dimensions</p> <p>Table 8: "Order codes": removed order codes LM258YPT and LM258AYPT; removed all order codes for devices with tube packing; added package code (NB) to DFN8 2x2 package.</p>
13-Nov-2015	13	<p>Updated document layout</p> <p>Updated name of the "DFN8 2x2 (NB) mm" package to "DFN8 2x2" everywhere in datasheet.</p> <p>Section 2: "Package pin connections": placed the package's pinout in this section and added note about exposed pad.</p> <p>Table 8: "Order codes": removed order codes LM258ST, LM358YPT, and LM358AYPT.</p>
24-Aug-2016	14	<p>Table 6: "DFN8 2x2 mechanical data": added typ. value for "L" dimension.</p>
22-Nov-2017	15	<p>Updated: related products on the cover page.</p> <p>Updated: <i>Section 3: "Absolute maximum ratings", Table 2: "Operating conditions", Section 4: "Electrical characteristics", Figure 6: "Voltage follower pulse response with VCC = 30 V" and Figure 7: "Input current".</i></p>

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