SAPIENZA
UNIVERSITÀ DI ROMA

FACOLTÀ DI INGEGNERIA DELL'INFORMAZIONE, INFORMATICA E STATISTICA

ESAMI DI STATO PER L'ABILITAZIONE ALLA PROFESSIONE DI INGEGNERE DELL'INFORMAZIONE

II SESSIONE – NOVEMBRE 2019

SEZIONE A

PROVA PRATICA

INGEGNERIA AUTOMATICA - CONTROL ENGINEERING LM-25

TRACCIA 1

Con riferimento ad un campo applicativo a scelta del candidato in cui il processo da controllare non sia modellizzabile, si progetti un sistema complessivo di controllo evidenziando, attraverso uno schema a blocchi opportunamente commentato, il processo da controllare, le funzionalità sensoristiche, le funzionalità attuative e le funzionzionalità di controllo.
Scelte specifiche progettuali in linea con il campo applicativo prescelto, si discutano le possibili metodologie di controllo evidenziandone vantaggi e svantaggi.

TRACCIA 2

Con riferimento ad un campo applicativo a scelta del candidato in cui il processo da controllare sia modellizzabile, si presenti tale modello e si progetti un sistema complessivo di controllo evidenziando, attraverso uno schema a blocchi opportunamente commentato, il processo da controllare, le funzionalità sensoristiche, le funzionalità attuative e le funzionzionalità di controllo.
Scelte specifiche progettuali in linea con il campo applicativo prescelto, si discutano le possibili metodologie di controllo evidenziandone vantaggi e svantaggi.

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II SESSIONE – NOVEMBRE 2019

SEZIONE A

PROVA PRATICA

INGEGNERIA ELETTRONICA LM-29

TRACCIA 1

Il candidato progetti l'interfaccia analogica di un sistema ottico finalizzato alla ricezione di segnali impulsivi con formato NRZ.
Segnale da trattare:

s(t)= Somme (i, 1, infinito) rect T (t-ti) A
T = 10 –50 ns
$t_{i+1} - t_i$ > 100ns
Pin = -30dBm

Caratteristiche dell'amplificatore e del fotorivelatore

Zin_0 < 50 Ohm
Zout_0 = 50 Ohm (entro 10 Ohm)
R =0,8 A/W (responsività fotodiodo)
Vout_min =10 mVpp (picco-picco)
La banda passante deve essere dimensionata in relazione al segnale da tratta (caso peggiore).

Il candidato è invitato a giustificare le scelte fatte nell'esecuzione del progetto.

Per i componenti attivi può utilizzare i datasheet forniti.

TRACCIA 2

II candidato progetti un amplificatore video per l’elaborazione di segnali impulsivi con le seguenti caratteristiche

BW > 100MHz
Av > 400 V/V
Zin = 50 Ohm (entro 5 Ohm)
Zout = 50 Ohm (entro 10 Ohm)
Delta_Av0/Av0 < 10%

Il candidato è invitato a giustificare le scelte fatte nell’esecuzione del progetto.

Per i componenti attivi può utilizzare i datasheet forniti.

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SEZIONE A

PROVA PRATICA

INGEGNERIA GESTIONALE

TRACCIA 1

Un investitore deve scegliere come far fruttare il proprio capitale che ammonta a 10000 Euro. Egli deve scegliere come suddividere l'investimento tra 5 tipologie distinte: conto corrente bancario, titoli di stato, obbligazioni, azioni e future. Ciascuno dei 5 investimenti proposti offre un tasso rendimento annuo (stimato o reale). Per diversificare il portafoglio, il budget (in Euro) destinato ad ogni investimento, se scelto, deve essere compreso tra un valore minimo ed un valore massimo, ovvero:

	tasso di rendimento	min. invest. (Euro)	max. invest. (Euro)
C/C bancario	2.5 %	0	1500
Titoli di Stato	6.5 %	0	5000
Obbligazioni	8.7 %	1000	5000
Azioni	18.7 %	500	4000
Future	11.5 %	0	4000

La somma degli investimenti in azioni ed obbligazioni non pu`o superare i 2/3 dell'intero capitale da investire.
1. Si costruisca un modello di Programmazione Matematica che massimizzi il rendimento annuo tenendo conto delle descritte restrizioni.

2. Dire a quale particolare classe di problemi di Programmazione Matematica appartiene il modello. Descrivere una metodologia in grado di risolvere efficientemente il precedente problema di ottimo.

3. Modificare il modello in modo da includere anche le seguenti restrizioni:
- non `e possibile investire contemporaneamente nel C/C bancario, nei Future e nei titoli di stato, solamente due dei tre;
- se si investe nelle obbligazioni allora si deve investire anche nei titoli di stato.

4. Dire a quale classe di problemi di Programmazione Matematica appartiene questo nuovo modello e descrivere, nuovamente, una metodologia in grado di risolverlo efficientemente.

TRACCIA 2

Il dirigente di un centro di calcolo deve stabilire quanti elaboratori acquistare. Il centro di calcolo `e aperto tutti i giorni della settimana (compresa la domenica). Tuttavia, per soddisfare le esigenze di calcolo del centro, il numero minimo di elaboratori che devono lavorare non `e costante per tutti i giorni ma varia in base al giorno considerato. Inoltre, per le particolari elaborazioni che svolge il centro, gli elaboratori lavorano per cinque giorni consecutivi e poi devono essere tenuti spenti per due giorni per manutenzione. Il dirigente, tenendo conto anche di altri vincoli

organizzativi, ha identificato come possibili turni di accensione degli elaboratori quelli riportati in tabella (un * indica
che l'elaboratore `e acceso in quel giorno, mentre un - l'elaboratore `e spento), insieme al numero minimo di elaboratori accesi necessari a garantire l'esigenze di calcolo:

	Lun	Mar	Mer	Gio	Ven	Sab	Dom
Turno 1	*	-	*	*	*	*	-
Turno 2	*	*	-	*	*	-	*
Turno 3	-	*	*	*	*	*	-
Turno 4	*	-	*	-	*	*	*
Turno 5	*	*	*	*	*	-	-
num.elaboratori	6	4	6	4	5	4	3

1. Formulare un modello di Programmazione Matematica che consenta di stabilire il minimo numero di elaboratori da acquistare per ciascun turno in modo da soddisfare le esigenze di servizio

2. Dire a quale particolare classe di problemi di Programmazione Matematica il modello appartiene. Descrivere una metodologia in grado di risolvere efficientemente il precedente problema di ottimo.

3. Modificare il modello in modo da includere anche le seguenti restrizioni:

- si vuole garantire il servizio utilizzando solamente 4 turni (cio`e si vuole acquistare elaboratori per assegnarli al piu` a 4 turni);
- si si decide di adottare il turno 5 allora si deve adottare necessariamente anche il turno 4.

4. Dire a quale classe di problemi di Programmazione Matematica appartiene questo nuovo modello e descrivere, nuovamente, una metodologia in grado di risolverlo efficientemente.

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SEZIONE A

PROVA PRATICA

Ingegneria Informatica LM-32

Traccia 1

Un centro commerciale aperto 12 ore al giorno necessita di un servizio di sicurezza che copra con dei turni adeguati tutte le 24 ore di ciascun giorno della settimana, perciò sia le ore in cui il centro commerciale è aperto, sia le ore in cui è chiuso. Ogni giornata consiste in 4 turni di 6 ore ciascuno. Si considerano diurni i due turni attivi durante le ore di apertura del centro commerciale, notturni i restanti due. Per i turni diurni, si richiede la presenza di 20 lavoratori a coprire ciascun turno. Per i restanti turni, sono necessari 5 lavoratori a turno. Il numero totale di lavoratori assunti nel supermercato è di 60 unità.
L'obiettivo del centro commerciale è lo sviluppo di un sistema informatico che si occupi dell'allocazione dei turni ai lavoratori secondo criteri di equità, considerando che: (1) i turni notturni sono considerati più gravosi di quelli diurni; (2) i turni durante le festività (domenica, Natale, Pasqua, ecc.) sono considerati i più gravosi in assoluto, sempre rispettando il vincolo al punto (1). Inoltre, per un lavoratore, devono essere evitati turni troppo ravvicinati fra loro (con meno di 12 ore fra l'uno e l'altro).

Il sistema informatico si appoggia ad un database centralizzato, che contiene tutti i dati necessari per garantire il servizio di allocazione dei turni. Ad esempio, il database contiene le informazioni anagrafiche dei lavoratori, il loro attuale stato di salute, le informazioni sui turni, e così via.
Il sistema informatico deve anche prevedere un'interfaccia web che consenta ai lavoratori di visionare i turni che gli sono stati assegnati (l'assegnazione avviene con 1 mese di anticipo), prevedendo la possibilità di segnalare in anticipo un'assenza in caso di ferie (almeno due settimane prima del turno) o di malattia (almeno 24 ore prima del turno previsto). In tal caso, il sistema informatico deve essere in grado di ri-allocare il personale per coprire il turno mancante.
Si richiede al candidato di progettare il sistema software descritto, svolgendo nello specifico i seguenti punti e motivando le sue scelte progettuali.

- Si esegua un'analisi dei requisiti, distinguendoli tra funzionali e non funzionali, preferibilmente usando diagrammi di casi d'uso UML.
- Assumendo che il database a disposizione sia relazionale, si costruisca una strutturazione delle informazioni memorizzate utilizzando un diagramma E-R, e si costruisca il corrispondente schema logico in SQL.
- Si progetti l'architettura del sistema, utilizzando preferibilmente diagrammi UML delle classi.
- Produrre in linguaggio SQL le interrogazioni necessarie per soddisfare i casi d'uso.
- Si sviluppi in un linguaggio di programmazione a scelta del candidato (Java, Python, C, ecc.), o eventualmente in pseudocodice, l'algoritmo che assegna i turni.

Per tutto ciò che non è specificato nel testo, il candidato formuli e giustifichi opportune ipotesi e svolga la prova sulla base di queste.

Traccia 2

L'azienda A vuole tenere traccia di un insieme di informazioni concernenti progetti software, descritte nel seguito. Ogni progetto ha un numero identificativo, un costo ed una durata (in giorni). Ogni progetto viene effettuato per un certo insieme di committenti (cioè aziende che incaricano A di effettuare il progetto), e ogni committente eroga, per ogni progetto, un relativo compenso all'azienda A.
Per ogni progetto, l'azienda A produce un insieme di schemi. Ogni schema viene sviluppato per uno ed un solo progetto, ed è caratterizzato da un numero, una versione ed il tempo (in giorni) impiegato per lo sviluppo. La combinazione di uno schema è unica nell'ambito del progetto per il quale lo schema è stato sviluppato.
Esistono esattamente tre tipi di schemi: class diagram, use case e sequence diagram. Per ognuno di essi interessa conoscere il/i progettista/i che ha/hanno concorso al loro sviluppo. Dei progettisti è di interesse conoscere il nome, il cognome, la data di nascita, il codice fiscale, e lo username e la password necessari per accedere all'applicazione di inserimento e modifica diagrammi.
In aggiunta, di ogni class diagram interessa il numero massimo di funzioni previste. Di ogni use case interessa la dimensione (espressa come un numero intero). Di ogni sequence diagram interessa il numero di classi coinvolte. Inoltre, ogni use case e sequence diagram si riferisce ad un solo class diagram che interessa conoscere. Infine, di ogni committente interessa il codice fiscale, la partita IVA, il numero di dipendenti, e il capitale sociale.
Al candidato si richiede di progettare un sistema informatico consistente in un'applicazione desktop che permette ad un progettista di navigare il contenuto informativo sopracitato e di svolgere le seguenti funzioni:

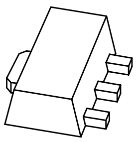
1. Registrarsi al sistema.
2. Effettuare login e logout.
3. Individuare i progetti maggiormente acceduti.
4. Creare un nuovo use case per un progetto.
5. Creare un nuovo sequence diagram per un progetto.
6. Creare un nuovo class diagram per un progetto.
7. Cancellare un diagramma esistente.
8. Visualizzare tutti i diagrammi sviluppati per un determinato progetto.

Sulla base delle specifiche di cui sopra si richiede di:

1. Produrre il diagramma UML dei casi d'uso dell'applicazione.
2. Disegnare l'architettura del sistema e discutere possibili strategie di deployment.

3. Scegliere tre funzionalità tra quelle descritte e dettagliarne la realizzazione.
4. Realizzare lo schema concettuale della base di dati (utilizzando un diagramma E-R) necessaria per lo sviluppo dell'applicazione.
5. Realizzare lo schema logico della base di dati in SQL.
6. Produrre le query SQL necessarie per implementare le tre funzionalità scelte al punto (3).

Per tutto quanto non specificato nel testo, il candidato formuli e giustifichi opportune ipotesi e svolga la prova sulla base di queste.



BFQ149

PNP 5 GHz wideband transistor

Rev. 03 — 28 September 2007 **Product data sheet**

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PNP 5 GHz wideband transistor — BFQ149

DESCRIPTION

PNP transistor in a SOT89 envelope. It is intended for use in UHF applications such as broadband aerial amplifiers (30 to 860 MHz) and in microwave amplifiers such as radar systems, spectrum analysers, etc., using SMD technology.

PINNING

PIN	DESCRIPTION
Code: FG	
1	emitter
2	collector
3	base

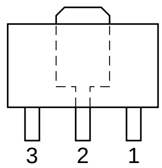


Fig.1 SOT89.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	open base	–	–	–15	V
I_C	DC collector current		–	–	–100	mA
P_{tot}	total power dissipation	up to T_s = 135 °C (note 1)	–	–	1	W
h_{FE}	DC current gain	I_C = –70 mA; V_{CE} = –10 V; T_j = 25 °C	20	50	–	
f_T	transition frequency	I_C = –75 mA; V_{CE} = –10 V; f = 500 MHz; T_j = 25 °C	4	5	–	GHz
G_{UM}	maximum unilateral power gain	I_C = –50 mA; V_{CE} = –10 V; f = 500 MHz; T_{amb} = 25 °C	–	12	–	dB
F	noise figure	I_C = –50 mA; V_{CE} = –10 V; R_s = 60 Ω; f = 500 MHz; T_{amb} = 25 °C	–	3.75	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–20	V
V_{CEO}	collector-emitter voltage	open base	–	–15	V
V_{EBO}	emitter-base voltage	open collector	–	–3	V
I_C	DC collector current		–	–100	mA
I_{CM}	peak collector current	f > 1 MHz	–	–150	mA
P_{tot}	total power dissipation	up to T_s = 135 °C (note 1)	–	1	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. T_s is the temperature at the soldering point of the collector tab.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	up to T_s = 135 °C (note 1)	40 K/W

Note

1. T_s is the temperature at the soldering point of the collector tab.

CHARACTERISTICS

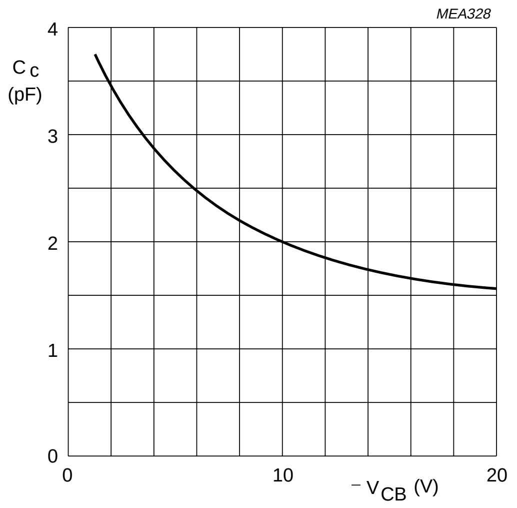
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = –10 V;	–	–	100	nA
h_{FE}	DC current gain	I_C = –70 mA; V_{CE} = –10 V	20	50	–	
f_T	transition frequency	I_C = –70 mA; V_{CE} = –10 V; f = 500 MHz; T_{amb} = 25 °C	4	5	–	GHz
C_c	collector capacitance	I_E = 0; V_{CB} = –10 V; f = 1 MHz	–	2	–	pF
C_e	emitter capacitance	I_C = 0; V_{EB} = –0.5 V; f = 1 MHz	–	4	–	pF
C_{re}	feedback capacitance	I_C = 0; V_{CE} = –10 V; f = 1 MHz	–	1.7	–	pF
G_{UM}	maximum unilateral power gain (note 1)	I_C = –50 mA; V_{CE} = –10 V; f = 500 MHz; T_{amb} = 25 °C	–	12	–	dB
F	noise figure	I_C = –50 mA; V_{CE} = –10 V; R_s = 60 Ω; f = 500 MHz; T_{amb} = 25 °C	–	3.75	–	dB

Note

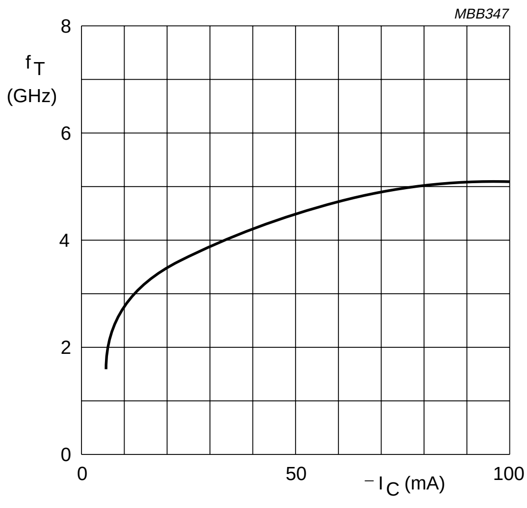
1. G_{UM} is the maximum unilateral power gain, assuming S_{12} is zero and

$$G_{UM} = 10 \log \frac{|S_{21}|^2}{\left(1 - |S_{11}|^2\right)\left(1 - |S_{22}|^2\right)} \text{dB}.$$



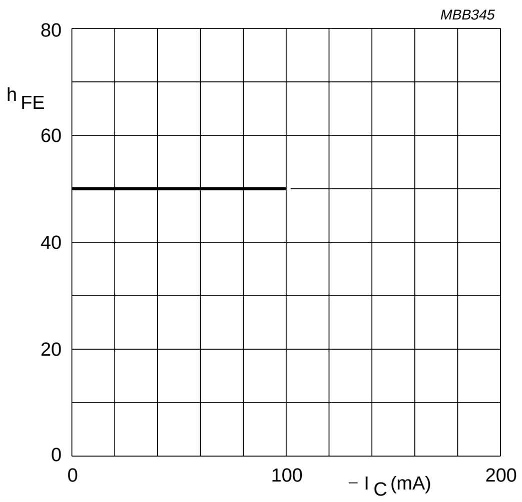
$I_E = 0$; f = 1 MHz; $T_j = 25$ °C.

Fig.2 Collector capacitance as a function of collector-base voltage.



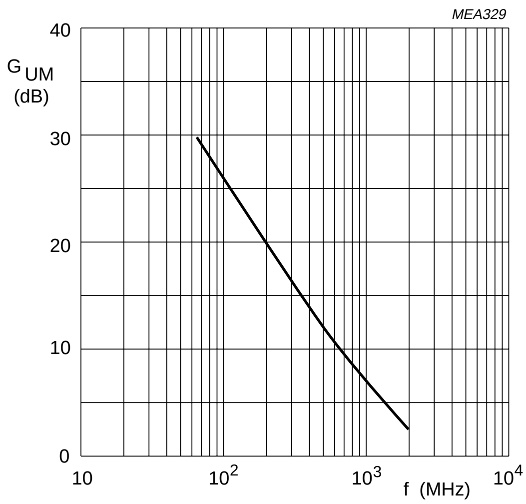
$V_{CE} = -10$ V; f = 500 MHz; $T_{amb} = 25$ °C.

Fig.3 Transition frequency as a function of collector current.



$V_{CE} = -10$ V; $T_j = 25$ °C.

Fig.4 DC current gain as a function of collector current.

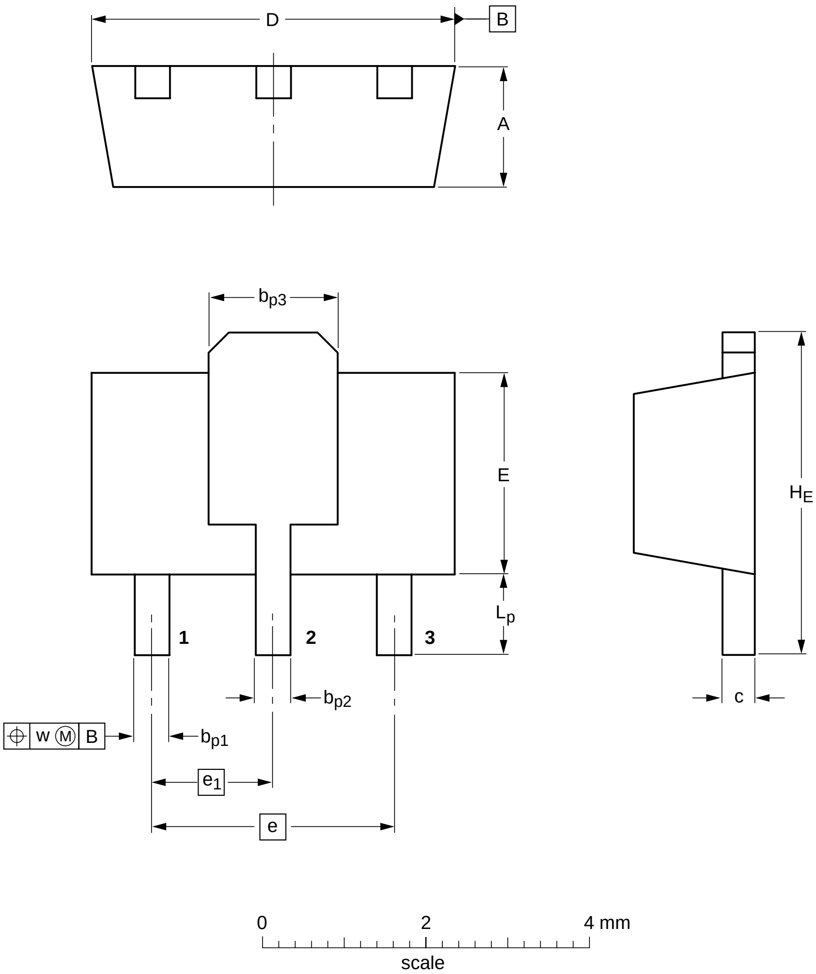


$I_c = -50$ mA; $V_{CE} = -10$ V; $T_{amb} = 25$ °C.

Fig.5 Maximum unilateral power gain as a function of frequency.

PACKAGE OUTLINE

Plastic surface-mounted package; collector pad for good heat transfer; 3 leads **SOT89**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_{p1}	b_{p2}	b_{p3}	c	D	E	e	e_1	H_E	L_p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			~~06-03-16~~ 06-08-29

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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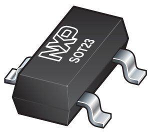
Revision history

Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BFQ149_N_3	20070928	Product data sheet	-	BFQ149_CNV_2
Modifications:	• Fig. 1 and package outline updated			
BFQ149_CNV_2	19950901	Product specification	-	-

Date of release: 28 September 2007
Document identifier: BFQ149_N_3



BFR520

NPN 9 GHz wideband transistor

Rev. 4 — 13 September 2011 **Product data sheet**

1. Product profile

1.1 General description

The BFR520 is an NPN silicon planar epitaxial transistor in a SOT23 plastic package.

1.2 Features and benefits

- High power gain
- Low noise figure
- High transition frequency
- Gold metallization ensures excellent reliability.

1.3 Applications

- RF front end wideband applications in the GHz range
  - Analog and digital cellular telephones
  - Cordless telephones (CT1, CT2, DECT, etc.)
  - Radar detectors
  - Pagers and satellite TV tuners (SATV)
  - Repeater amplifiers in fiber-optic systems.

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CBO}	collector-base voltage			-	-	20	V
V_{CES}	collector-emitter voltage	R_{BE} = 0 Ω		-	-	15	V
I_C	collector current (DC)			-	-	70	mA
P_{tot}	total power dissipation	up to T_{sp} = 97 °C	[1]	-	-	300	mW
h_{FE}	DC current gain	I_C = 20 mA; V_{CE} = 6 V		60	120	250	
C_{re}	feedback capacitance	I_C = i_c = 0 A; V_{CB} = 6 V; f = 1 MHz		-	0.4	-	pF
f_T	transition frequency	I_C = 20 mA; V_{CE} = 6 V; f = 1 GHz		-	9	-	GHz
G_{UM}	maximum unilateral power gain	I_C = 20 mA; V_{CE} = 6 V; T_{amb} = 25 °C					
		f = 900 MHz		-	15	-	dB
		f = 2 GHz		-	9	-	dB

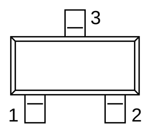
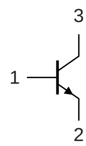
Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\|s_{21}\|^2$	insertion power gain	I_C = 20 mA; V_{CE} = 6 V; T_{amb} = 25 °C; f = 900 MHz	13	14	-	dB
NF	noise figure	$\Gamma_s = \Gamma_{opt}$; T_{amb} = 25 °C				
		I_C = 5 mA; V_{CE} = 6 V; f = 900 MHz	-	1.1	1.6	dB
		I_C = 20 mA; V_{CE} = 6 V; f = 900 MHz	-	1.6	2.1	dB
		I_C = 5 mA; V_{CE} = 8 V; f = 2 GHz	-	1.9	-	dB

[1] T_{sp} is the temperature at the soldering point of the collector tab.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	base		 sym021
2	emitter		
3	collector		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BFR520	-	plastic surface mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking

Type number	Marking code[1]
BFR520	32*

[1] * = p: Made in Hong Kong
* = t: Made in Malaysia
* = W: Made in China.

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	20	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0\ \Omega$		-	15	V
V_{EBO}	emitter-base voltage	open collector		-	2.5	V
I_C	collector current (DC)			-	70	mA
P_{tot}	total power dissipation	up to T_{sp} = 97 °C	[1]	-	300	mW
T_{stg}	storage temperature			–65	150	°C
T_j	junction temperature			-	175	°C

[1] T_{sp} is the temperature at the soldering point of the collector tab.

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j\text{-}s)}$	thermal resistance from junction to soldering point		[1]	260	K/W

[1] T_{sp} is the temperature at the soldering point of the collector tab.

7. Characteristics

Table 7. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CBO}	collector cut-off current	I_E = 0 A; V_{CB} = 6 V		-	-	50	nA
h_{FE}	DC current gain	I_C = 20 mA; V_{CE} = 6 V		60	120	250	
C_e	emitter capacitance	$I_C = i_c$ = 0 A; V_{EB} = 0.5 V; f = 1 MHz		-	1	-	pF
C_c	collector capacitance	$I_E = i_e$ = 0 A; V_{CB} = 6 V; f = 1 MHz		-	0.5	-	pF
C_{re}	feedback capacitance	I_C = 0 A; V_{CB} = 6 V; f = 1 MHz		-	0.4	-	pF
f_T	transition frequency	I_C = 20 mA; V_{CE} = 6 V; f = 1 GHz		-	9	-	GHz
G_{UM}	maximum unilateral power gain	I_C = 20 mA; V_{CE} = 6 V; T_{amb} = 25 °C	[1]				
		f = 900 MHz		-	15	-	dB
		f = 2 GHz		-	9	-	dB
$\|s_{21}\|^2$	insertion power gain	I_C = 20 mA; V_{CE} = 6 V; T_{amb} = 25 °C; f = 900 MHz		13	14	-	dB

Table 7. Characteristics *...continued*

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
NF	noise figure	$\Gamma_s = \Gamma_{opt}$; V_{CE} = 6 V; T_{amb} = 25 °C					
		I_C = 5 mA; f = 900 MHz		-	1.1	1.6	dB
		I_C = 20 mA; f = 900 MHz		-	1.6	2.1	dB
		I_C = 5 mA; f = 2 GHz		-	1.9	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	I_C = 20 mA; V_{CE} = 6 V; R_L = 50 Ω; T_{amb} = 25 °C; f = 900 MHz		-	17	-	dBm
ITO	third order intercept point		[2]	-	26	-	dBm

[1] G_{UM} is the maximum unilateral power gain, assuming s_{12} is zero and

$$G_{UM} = 10\ log \frac{|s_{21}|^2}{(1-|s_{11}|^2)(1-|s_{22}|^2)}\ dB.$$

[2] I_C = 20 mA; V_{CE} = 6 V; R_L = 50 Ω; T_{amb} = 25 °C; f_p = 900 MHz; f_q = 902 MHz
Measured at $f_{(2p-q)}$ = 898 MHz and $f_{(2q-p)}$ = 904 MHz.

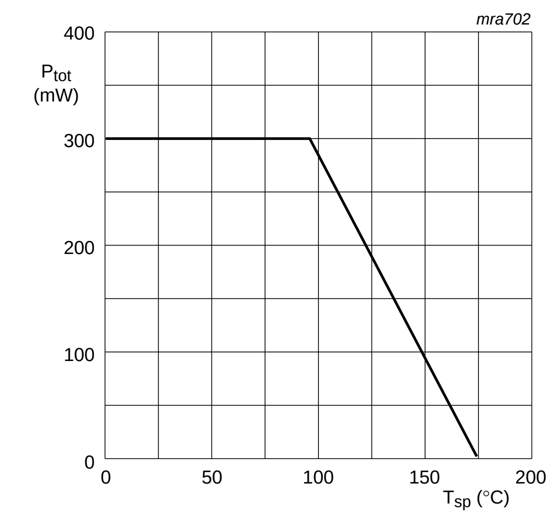
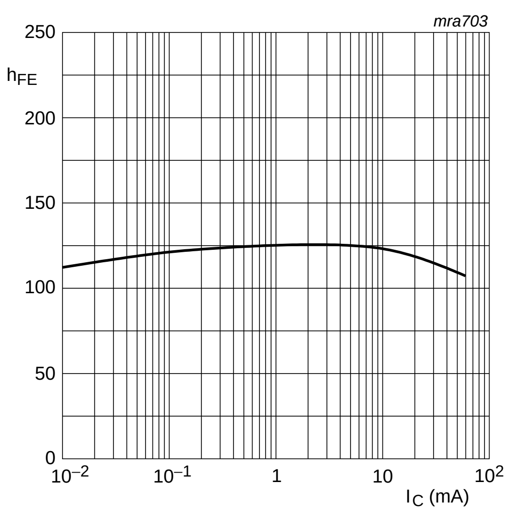
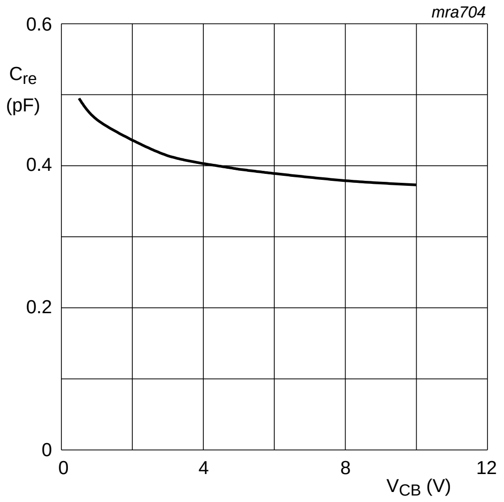


Fig 1. Power derating curve.



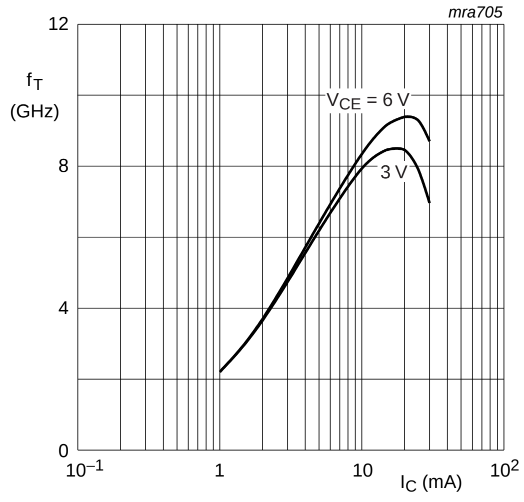
V_{CE} = 6 V.

Fig 2. DC current gain as a function of collector current.



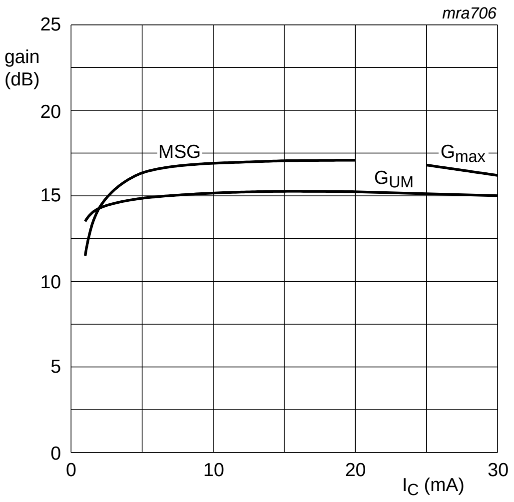
I_C = 0 A; f = 1 MHz.

Fig 3. Feedback capacitance as a function of collector-base voltage.



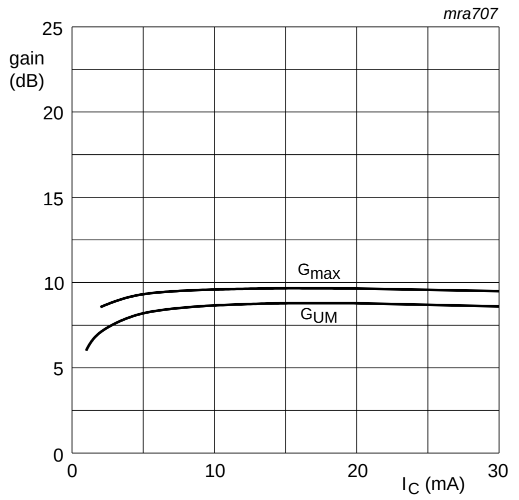
T_{amb} = 25 °C; f = 1 GHz.

Fig 4. Transition frequency as a function of collector current.



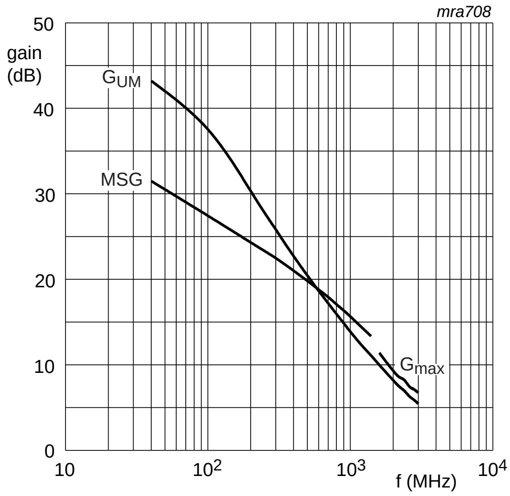
V_{CE} = 6 V; f = 900 MHz.

Fig 5. Gain as a function of collector current; f = 900 MHz.



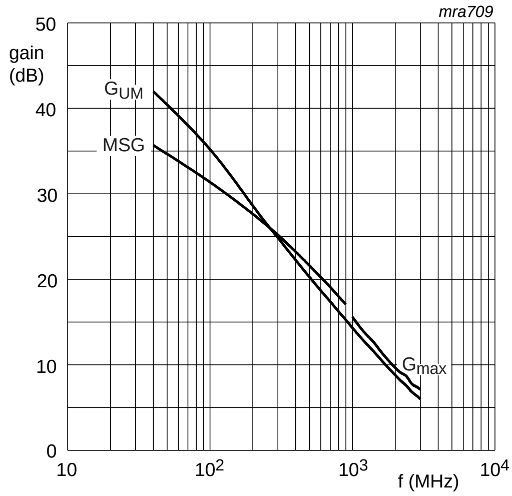
V_{CE} = 6 V; f = 2 GHz.

Fig 6. Gain as a function of collector current; f = 2 GHz.



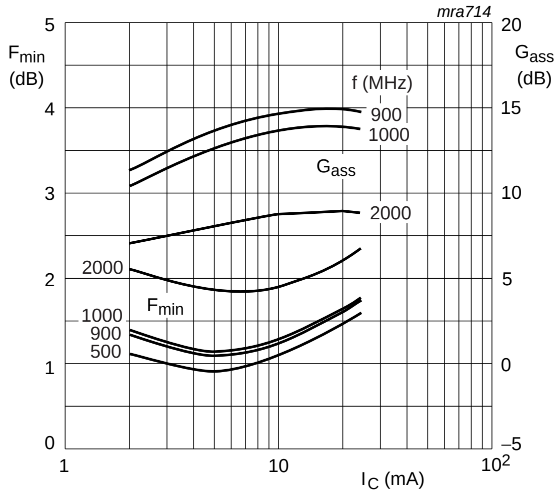
V_{CE} = 6 V; I_C = 5 mA.

Fig 7. Gain as a function of frequency; I_C = 5 mA.



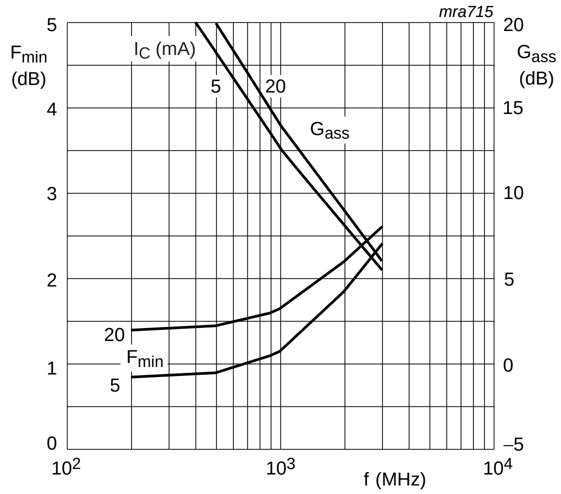
V_{CE} = 6 V; I_C = 20 mA.

Fig 8. Gain as a function of frequency; I_C = 20 mA.



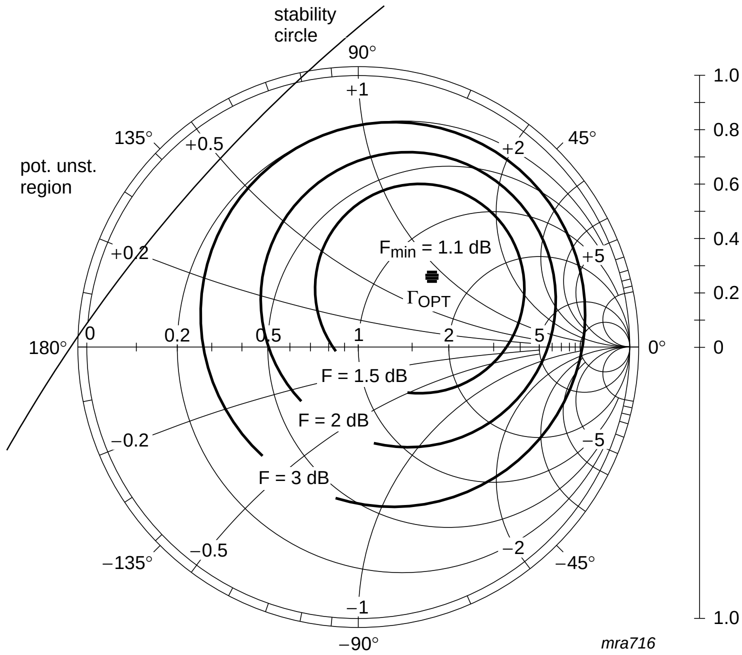
V_{CE} = 6 V.

Fig 9. Minimum noise figure and associated available gain as functions of collector current.



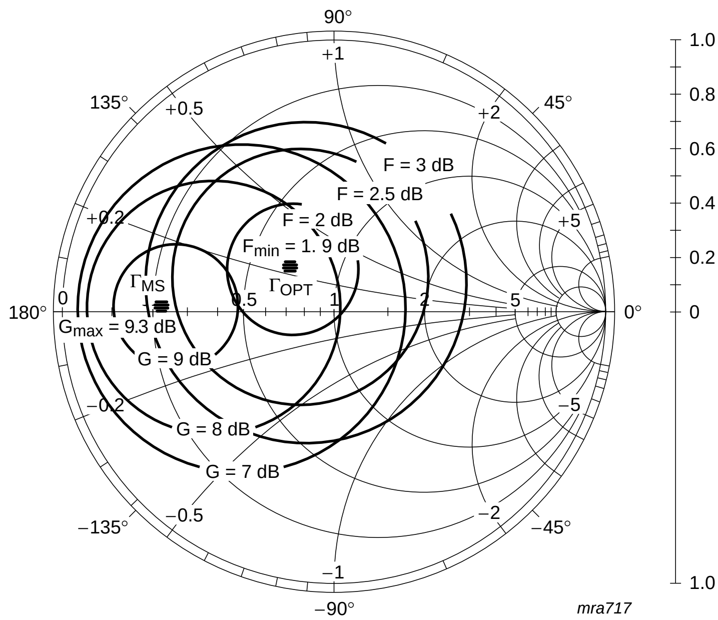
V_{CE} = 6 V.

Fig 10. Minimum noise figure and associated available gain as functions of frequency.



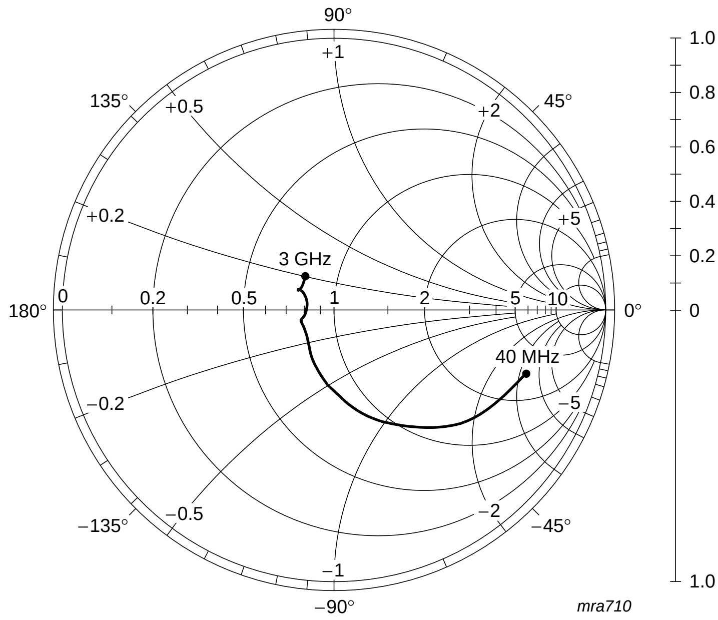
Z_o = 50 Ω; V_{CE} = 6 V; I_C = 5 mA; f = 900 MHz.

Fig 11. Noise circle figure; f = 900 MHz.



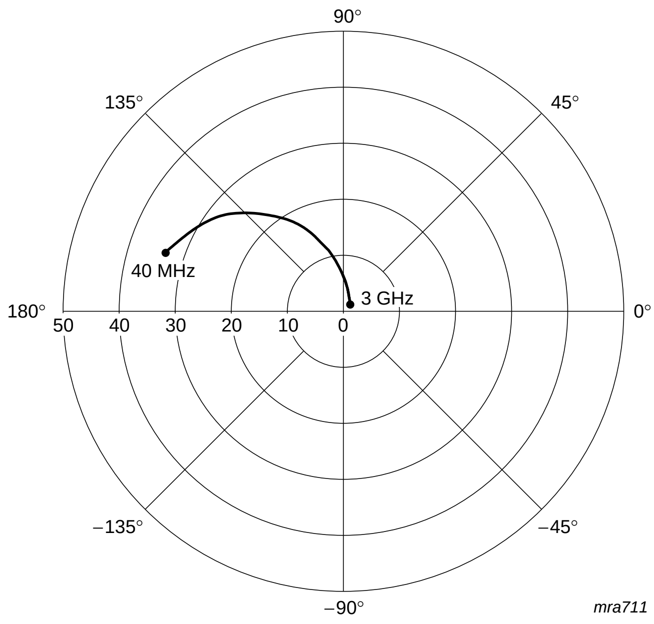
Z_o = 50 Ω; V_{CE} = 6 V; I_C = 5 mA; f = 2000 MHz.

Fig 12. Noise circle figure; f = 2000 MHz.



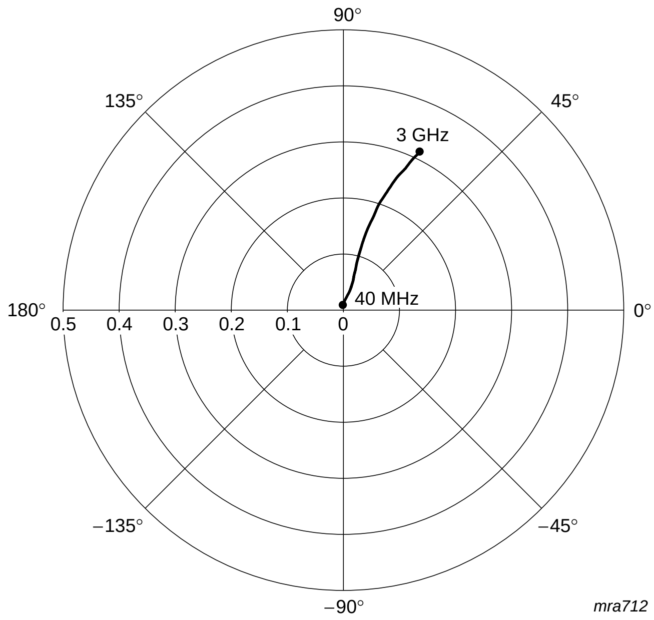
V_{CE} = 6 V; I_C = 20 mA; Z_o = 50 Ω.

Fig 13. Common emitter input reflection coefficient (s_{11}).



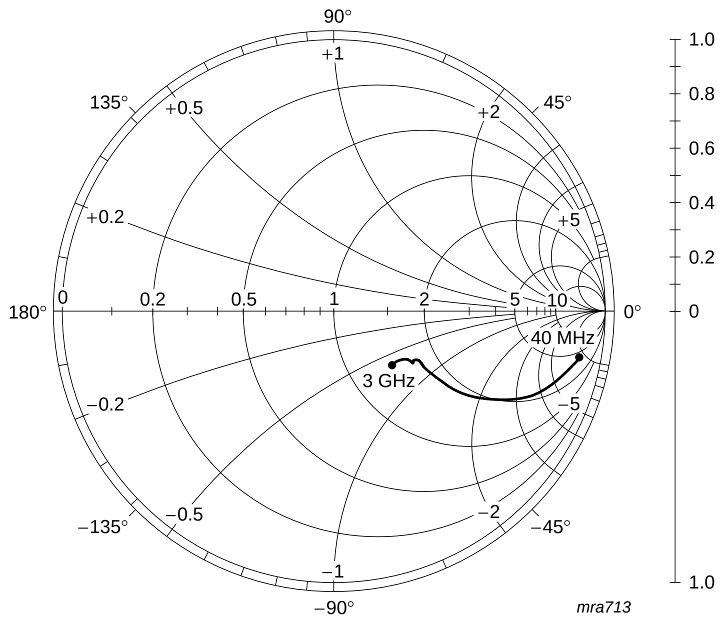
V_{CE} = 6 V; I_C = 20 mA.

Fig 14. Common emitter forward transmission coefficient (s_{21}).



V_{CE} = 6 V; I_C = 20 mA.

Fig 15. Common emitter reverse transmission coefficient (s_{12}).

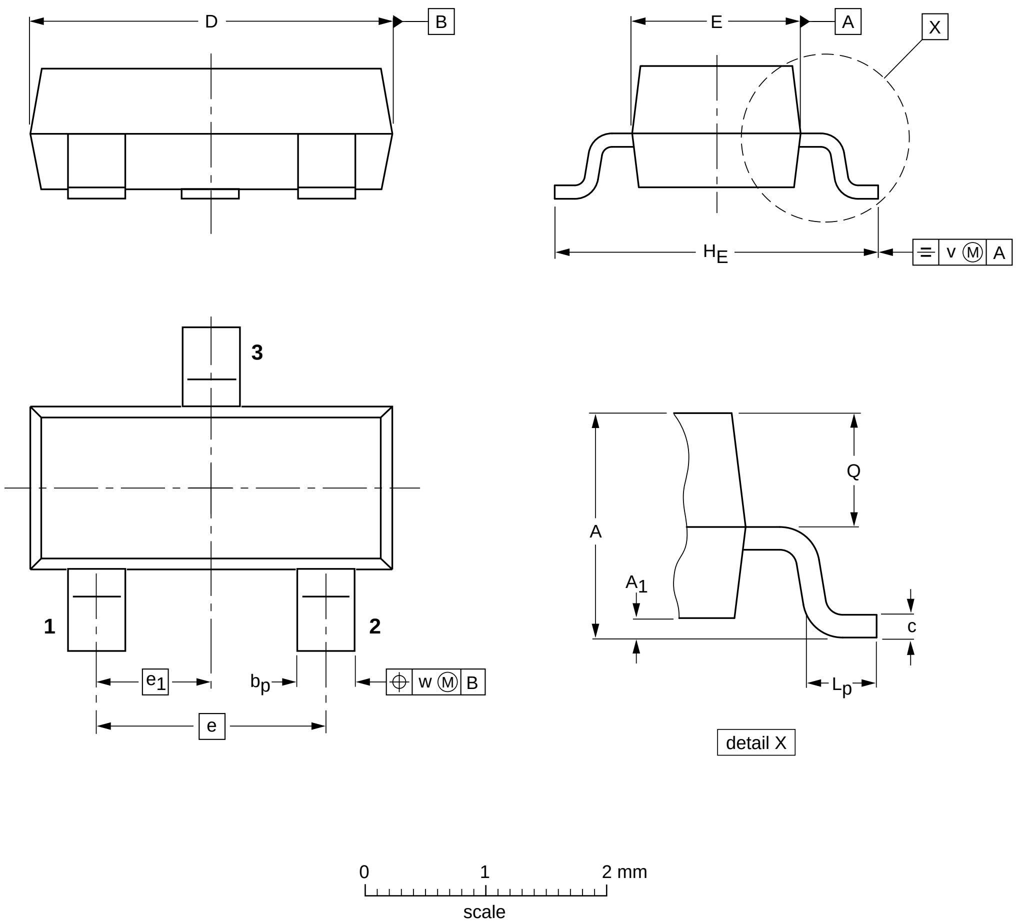


V_{CE} = 6 V; I_C = 20 mA; Z_o = 50 Ω.

Fig 16. Common emitter output reflection coefficient (s_{22}).

8. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~04-11-04~~ 06-03-16

Fig 17. Package outline SOT23 (TO-236AB).

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BFR520 v.4	20110913	Product data sheet	-	BFR520 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package outline drawings have been updated to the latest version.			
BFR520 v.3 (9397 750 13397)	20040901	Product data sheet	-	BFR520_CNV v.2
BFR520_CNV v.2	19971204	Product specification	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contact information

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12. Contents

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Date of release: 13 September 2011
Document identifier: BFR520

DATA SHEET

BFT92
PNP 5 GHz wideband transistor

Product specification

November 1992

PNP 5 GHz wideband transistor — BFT92

DESCRIPTION

PNP transistor in a plastic SOT23 envelope.

It is primarily intended for use in RF wideband amplifiers, such as in aerial amplifiers, radar systems, oscilloscopes, spectrum analyzers, etc. The transistor features low intermodulation distortion and high power gain; due to its very high transition frequency, it also has excellent wideband properties and low noise up to high frequencies.

NPN complements are BFR92 and BFR92A.

PINNING

PIN	DESCRIPTION
Code: W1p	
1	base
2	emitter
3	collector

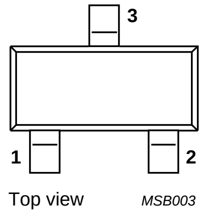


Fig.1 SOT23.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–20	V
V_{CEO}	collector-emitter voltage	open base	–	–15	V
I_C	DC collector current		–	–25	mA
P_{tot}	total power dissipation	up to T_s = 95 °C; note 1	–	300	mW
f_T	transition frequency	I_C = –14 mA; V_{CE} = –10 V; f = 500 MHz	5	–	GHz
C_{re}	feedback capacitance	I_C = –2 mA; V_{CE} = –10 V; f = 1 MHz	0.7	–	pF
G_{UM}	maximum unilateral power gain	I_C = –14 mA; V_{CE} = –10 V; f = 500 MHz; T_{amb} = 25 °C	18	–	dB
F	noise figure	I_C = –5 mA; V_{CE} = –10 V; f = 500 MHz; T_{amb} = 25 °C	2.5	–	dB
d_{im}	intermodulation distortion	I_C = –14 mA; V_{CE} = –10 V; R_L = 75 Ω; V_o = 150 mV; T_{amb} = 25 °C; $f_{(p+q-r)}$ = 493.25 MHz	–60	–	dB

Note

1. T_s is the temperature at the soldering point of the collector tab.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–20	V
V_{CEO}	collector-emitter voltage	open base	–	–15	V
V_{EBO}	emitter-base voltage	open collector	–	–2	V
I_C	DC collector current		–	–25	mA
I_{CM}	peak collector current	f > 1 MHz	–	–35	mA
P_{tot}	total power dissipation	up to T_s = 95 °C; note 1	–	300	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	up to T_s = 95 °C; note 1	260 K/W

Note

1. T_s is the temperature at the soldering point of the collector tab.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

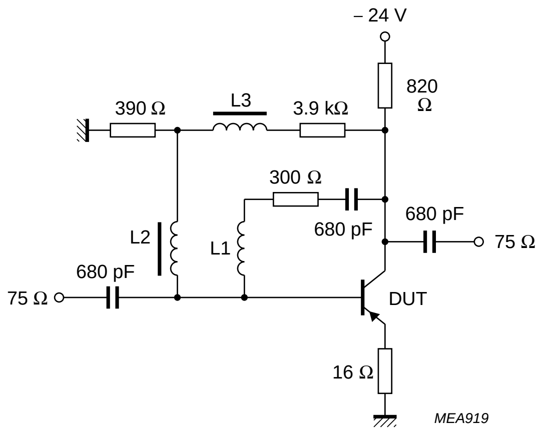
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = –10 V;	–	–	–50	nA
h_{FE}	DC current gain	I_C = –14 mA; V_{CE} = –10 V	20	50	–	
f_T	transition frequency	I_C = –14 mA; V_{CE} = –10 V; f = 500 MHz	–	5	–	GHz
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = –10 V; f = 1 MHz	–	0.75	–	pF
C_e	emitter capacitance	$I_C = i_c$ = 0; V_{EB} = –0.5 V; f = 1 MHz	–	0.8	–	pF
C_{re}	feedback capacitance	I_C = –2 mA; V_{CE} = –10 V; f = 1 MHz	–	0.7	–	pF
G_{UM}	maximum unilateral power gain (note 1)	I_C = –14 mA; V_{CE} = –10 V; f = 500 MHz; T_{amb} = 25 °C	–	18	–	dB
F	noise figure	I_C = –5 mA; V_{CE} = –10 V; f = 500 MHz; T_{amb} = 25 °C	–	2.5	–	dB
V_o	output voltage	note 2	–	150	–	mV

Notes

1. G_{UM} is the maximum unilateral power gain, assuming S_{12} is zero and

$$G_{UM} = 10 \log \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \text{dB}.$$

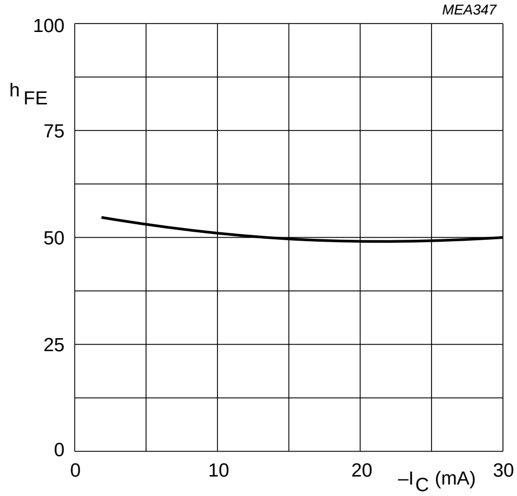
2. d_{im} = –60 dB (DIN 45004B); I_C = –14 mA; V_{CE} = –10 V; R_L = 75 Ω;
   $V_p = V_o$ at d_{im} = –60 dB; f_p = 495.25 MHz;
   $V_q = V_o$ –6 dB; f_q = 503.25 MHz;
   $V_r = V_o$ –6 dB; f_r = 505.25 MHz;
   measured at $f_{(p+q-r)}$ = 493.25 MHz.



L2 = L3 = 5 μH Ferroxcube choke, catalogue number 3122 108 20150.

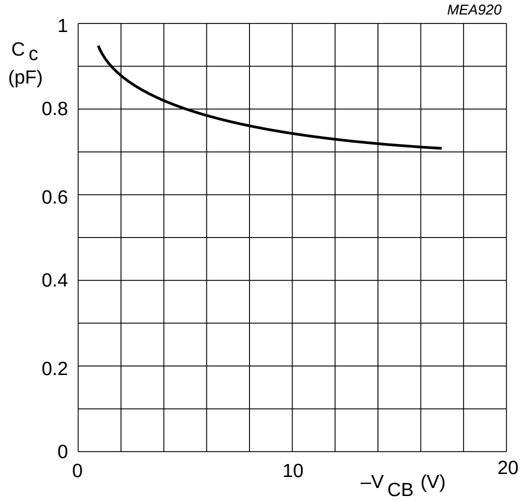
L1 = 4 turns 0.35 mm copper wire; winding pitch 1 mm; internal diameter 4 mm.

Fig.2 Intermodulation distortion test circuit.



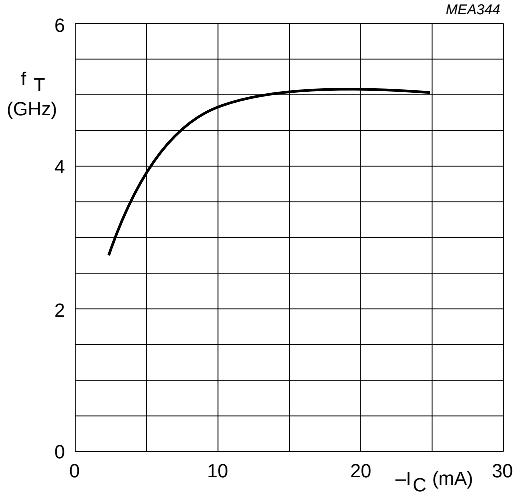
V_{CE} = –10 V; T_j = 25 °C.

Fig.3 DC current gain as a function of collector current.



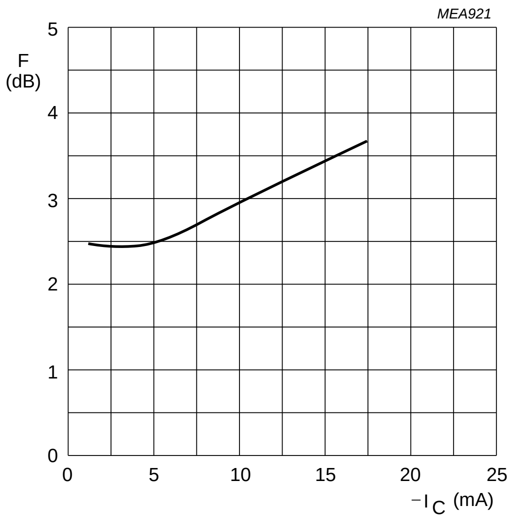
$I_E = i_e = 0$; f = 1 MHz; T_j = 25 °C.

Fig.4 Collector capacitance as a function of collector-base voltage.



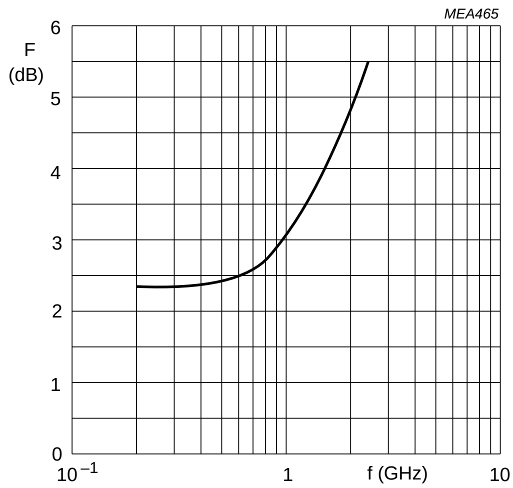
V_{CE} = –10 V; f = 500 MHz; T_j = 25 °C.

Fig.5 Transition frequency as a function of collector current.



V_{CE} = –10 V; Z_s = opt.; f = 500 MHz; T_{amb} = 25 °C.

Fig.6 Minimum noise figure as a function of collector current.

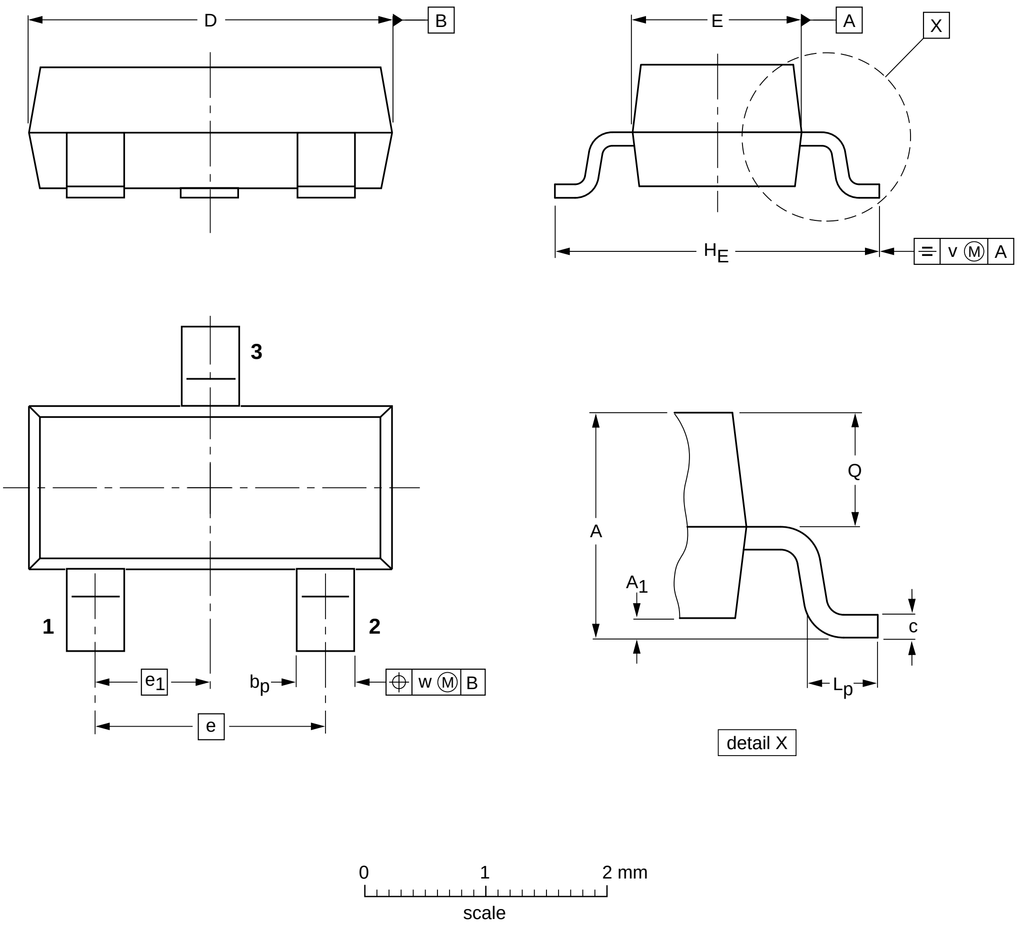


I_c = –2 mA; V_{CE} = –10 V; Z_s = opt.; T_{amb} = 25 °C.

Fig.7 Minimum noise figure as a function of frequency.

PACKAGE OUTLINE

Plastic surface-mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~04-11-04~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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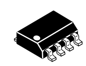


CASE 751–05, STYLE 1
(SO–8)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	–30	V
Collector–Base Voltage	V_{CBO}	–30	V
Emitter–Base Voltage	V_{EBO}	–3.0	V
Collector Current — Continuous	I_C	–500	mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

DEVICE MARKING

MRF5583 = 5583

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Storage Temperature	T_{stg}	150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

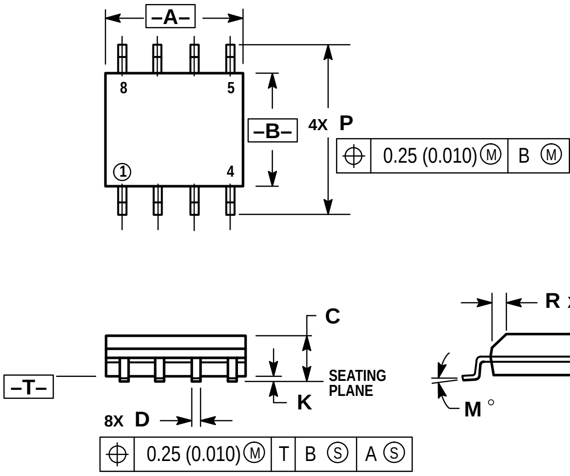
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

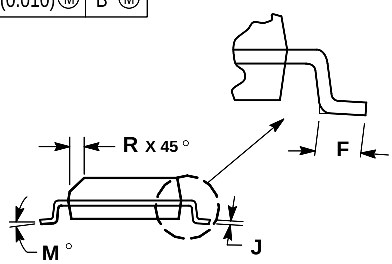
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = –10 mA)	$V_{(BR)CEO}$	–30	—	—	V
Collector–Base Breakdown Voltage (I_C = –10 μA)	$V_{(BR)CBO}$	–30	—	—	V
Emitter–Base Breakdown Voltage (I_E = –100 μA)	$V_{(BR)EBO}$	–3	—	—	V
Collector Cutoff Current (V_{CB} = –20 V)	I_{CBO}	—	—	–1.0	μA
Emitter Cutoff Current (V_{EB} = –2.0 V)	I_{EBO}	—	—	–0.5	μA
ON CHARACTERISTICS					
DC Current Gain (I_C = –40 mA, V_{CE} = –2.0 V) (I_C = –100 mA, V_{CE} = –2.0 V) (I_C = –300 mA, V_{CE} = –5.0 V)	h_{FE}	20 25 15	— — —	— 100 —	—
Collector–Emitter Saturation Voltage (I_C = –100 mA, I_B = –10 mA)	$V_{CE(sat)}$	—	—	0.8	V
Base–Emitter On Voltage (I_C = –100 mA, V_{CE} = –2.0 V)	$V_{BE(on)}$	—	—	1.8	V
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = –35 mA, V_{CE} = –15 V, f = 100 MHz)	f_T	—	2100	—	MHz
Insertion Gain (V_{CE} = –15 V, I_C = –35 mA, f = 250 MHz)	$|S_{21}|^2$	12.5	15.5	—	dB

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	φ	$\|S_{21}\|$	φ	$\|S_{12}\|$	φ	$\|S_{22}\|$	φ
–15	–35	10	0.47	–57	64.7	155	0.01	60	0.83	–26
		30	0.59	–116	42.2	126	0.02	44	0.56	–58
		50	0.63	–140	28.8	113	0.02	39	0.39	–74
		70	0.64	–151	21.4	105	0.02	42	0.30	–82
		100	0.65	–161	15.4	97	0.02	45	0.24	–80
		300	0.67	179	5.23	79	0.05	58	0.13	–109
		500	0.67	168	3.11	66	0.07	60	0.20	–114
		700	0.67	160	2.24	57	0.09	60	0.24	–116
		1000	0.66	146	1.54	44	0.13	60	0.30	–123

Table 1. Common Emitter S–Parameters

PACKAGE DIMENSIONS





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

CASE 751–05
ISSUE M

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